Deliverable – D4.5

Final benchmarking towards evolving wideband communication and sensing including identification of limiting factors and a technology roadmap

Project acronym	SEQUENCE
Project number	871764
Project title	Cryogenic 3D Nanoelectronics (Sense and Readout Electronics Cryogenically Integrated for QUantum ENhanced Computation and Evolving Communication)

Document Properties	
Nature of Document	Report
Work Package	WP4 - Communication and Sensing
Task Leader	Beneficiary 8 – CTA
Authors	Lars Ohlsson Fhager, Lars-Erik Wernersson (ULUND) Fabian Thome (IAF) Simon Olson, Tobias Tired (CTA) Didier Belot, Alexandre Siligaris, Vincent Puyal (LETI)
Version	1.2
Status of Document	Final
Due Date of deliverable	M40
Actual delivery date	M43
Dissemination Level	PU

Document history			
Version	Date	Author	Status – Reason for change
0.0	2022-12-06	Simon Olson	Template
1.0	2023-06-02	All authors	Collated input from all partners
1.1	2023-06-22	Lars Ohlsson Fhager	Merging parts
1.2	2023-06-30	All authors	Final revision

Release approval			
Version	Date	Name and organisation	Role
1.2	2023-06-30	Lars-Erik Wernersson (ULUND)	PC

The project has received funding from the European Union's Horizon 2020 research and innovation programme under Grant agreement number 871764 (SEQUENCE).

Contents

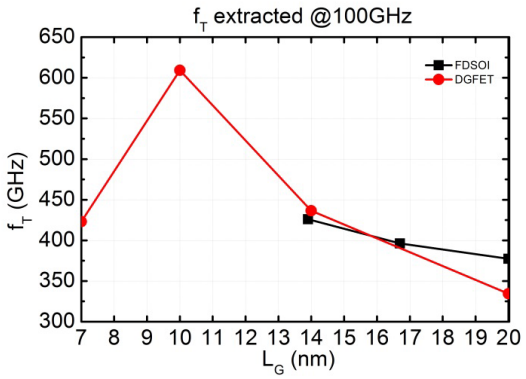
1 Introduction

This document reports the circuit design activities in WP4, revolving around synergistic connections from quantum electronics towards Communication and Sensing. The **added value brought by the SEQUENCE consortium** is first highlighted in relation to the International Roadmap for Devices and Systems (IRDS) 2022 reports (https://irds.ieee.org/editions/2022); specifically "IRDS 2022: CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING" and "IRDS 2022: OUTSIDE SYSTEM CONNECTIVITY". In this introductory section, the considerations of device trends are evaluated. The rest of the report is organized with close consideration of task descriptions in the SEQUENCE proposal to facilitate the review process.

1.1 Devices Trends:

MOSFET:

"The 2020 roadmap technology plots reflect the RF and analog performance metrics needed to support the technology roadmap developed by the IRDS More Moore IFT in 2017. The RF-AMS performance metrics for CMOS devices have been restricted to peak fT and peak gm and have been calibrated on recent averaged measured data in the 28 nm, 22 nm, and 16 nm nodes. Compared to previous editions of the ITRS, the new fT data provide a more realistic view of the projected high frequency performance of future MOSFET devices down to physical gate lengths of 7 nm. They indicate the degradation in fT and gm at gate lengths below 10 nm as a result of mobility degradation caused by surface scattering at the gate oxide interface, and due to the ever-thinner silicon body. As can be observed, the double gate of the FinFET results in higher transconductance but also higher capacitive parasitic elements compared to the single-gate FDSOI MOSFETs."

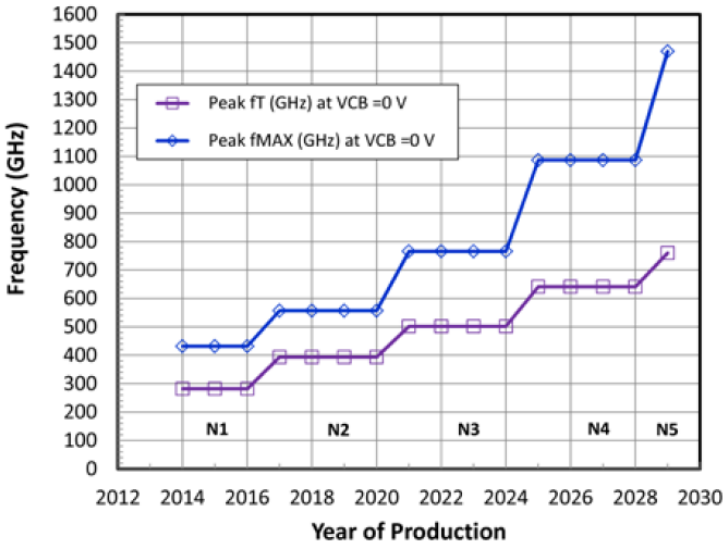


IRDS 2022 Figure: CMOS Roadmap for Peak fT vs. Physical Gate Length for FDSOI and Double-gate (FinFET) MOSFETs

III-V/ Si nanowire FET is one of the tracks followed by SEQUENCE, which could outcome to an improvement of this Ft limitation. The other approach is to use Silicon FDSOI CMOS at its optimal temperature which is between 30°K and 77°K, and digital building block have been designed to evaluate the interest to do computer in this temperature range. In addition, as it was mentioned by IRDS, a possible computing application can be developed at cryogenic temperature where CMOS Ft is largely better than obtained at room temperature.

Group IV HBT:

"The roadmap for SiGe heterojunction bipolar transistors (HBTs) and associated benchmark circuits at mm-wave frequencies has been based since 2013 on a seamless set of TCAD device simulation tools in order to obtain consistent compact model parameters for the complete transistor structure used in the respective circuit simulations The data (including the minimum emitter width WE, and all electrical performance parameters such as fT, BVCEO, BVCBO, JC at peak fT, NFMIN, MAG etc.) in the 2015 Technology Requirements Tables for high-speed NPN transistors, have been shifted by one-year, as shown in Table OSC-16 of the IRDS report. Performance plateaus have been assumed to last four years and are linked to applications and the foregoing system drivers. The benchmark circuits for LNA, PA, VCO, and current-mode-logic-based (CML) ring-oscillator (RO) have been manually optimized for each technology node and a variety of commercially relevant frequencies. The most recent result for a prototyping process corresponds closely to the performance predicted for node N3."



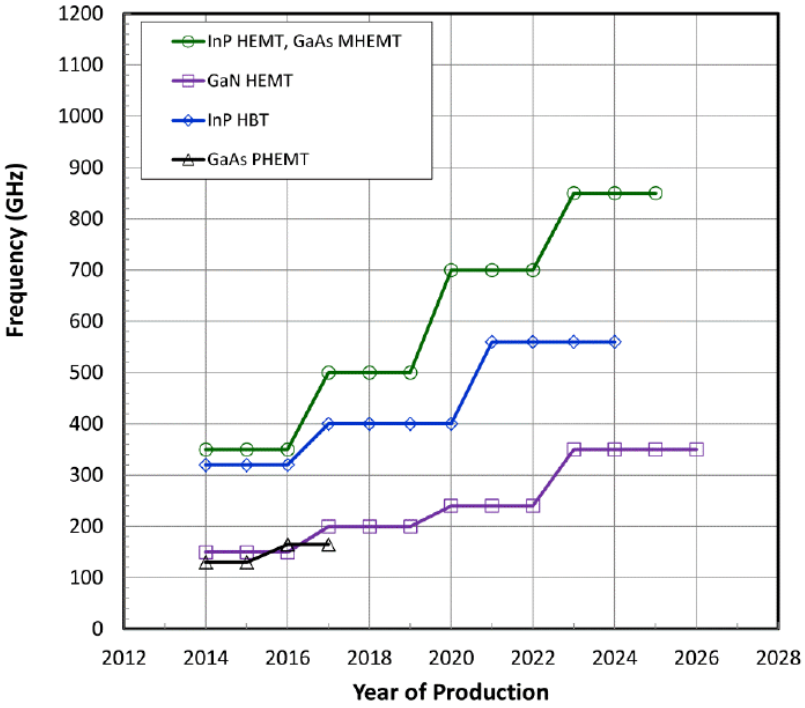
IRDS 2022 Figure: High Speed SiGe HBT fT and fMAX Roadmap vs. Year of Production

SEQUENCE project does not address SiGe HBT, and the consortium has done benchmarking actions through Workwhops organized at EuMW and IMS. These devices are integrated in the global cryogenic roadmap and will be studied by part of the Consortium which continue working in the future KDT Semi-Cryo RIA program. SiGe HBT can compete in the mmWave to THz communication and the Qubit readout functions.

III-V FET and Bipolar:

"We have assumed "production" implies that at least one company offers products with "data sheets" or that the technology is available for custom designs from one or more companies as a foundry service. The productions dates for all technologies have been shifted by one year later. The 'pull' for these technologies partly drives this shift. The III-V roadmap truncates at the following expected ends of scaling: GaAs pseudomorphic high electron mobility transistor (PHEMT) in 2015, GaAs power metamorphic high electron mobility transistor (MHEMT) in 2020, and InP power high electron mobility transistor (HEMT) in 2016. However, it is expected that low noise GaAs MHEMT and InP HEMT, InP HBT, and GaN HEMT will continue with physical scaling. The FoMs depend on technology and will include: fT, fMAX, gm, and VBD; power, gain, and efficiency at 10, 24, 60, 94, 140, and 220 GHz; NFMIN and GA at 10, 24, 60, and 94 GHz; LNA NF and GA at 140 and 220 GHz. As mentioned previously, RF and AMS front-end components are a growing part of the semiconductor industry. However, this has

divided the III-V technology landscape into two groups, one dominated by the large volume consumer market and the other dominated by low volume specialty markets. Within the III-V technology landscape, the large volume consumer driven market is best represented by GaAs HBT power amplifiers for cellular communications. The low volume specialty markets to which InP HEMT, InP HBT, and GaN HEMT presently belong also suffer from the slow pace of the slow transition to mass production due to low product volumes. Many of these technologies are driven by noncommercial needs and experience sudden leaps in performance only when government funding becomes available."



IRDS 2022 Figure: III-V Roadmap for fT

For future telecom generation, the need of THz Fmax process will become more and more vital, as High Data rate communication will need wider and wider bandwidth, which could be provided at very high carrier frequency, above 100GHz and at the end of the decade up to 300GHz. The main challenge will be to propose III-V / Si processes reducing the cost of the mmWaves and Sub-THz PA/LNA and Switches functions. In the same time, multi Qubits read functions will need wide band LNAs working at 1 to 4 °K, these ultra-low noise figure amplifiers will benefit from high Ft, so III-V processes based on InP and GaAs can bring possible solutions. In SEQUENCE, InGaAS MHEMT LNAs for Qubit readout, and space communications, and InGaAs Nanowires LNAs for mmWaves and Sub-THz terrestrial communications are developed.

2 Wireless Wideband Communication and Sensing at Room Temperature

2.1 Multi-Frequency Signal Generation (ST 4.1.1)

LETI has presented a multi-tone generator circuit for the 2-4.5 GHz range. Table 2.1 shows a comparison of the multi-tone generator circuit fabricated in CMOS45RFSOI technology with two other works presenting multi-tone frequency generators. The total chip area is 2.25 mm^2 of which 0.27 mm^2 corresponds to the core circuit (not including pads). The implemented circuit consumes 84.4 mW for

α = 0.2. It is high due to the DCC and the injection transistors presence but has been reduced on similar circuits, by optimizing the injection transistors sizing, designed for another application. This means that we can drastically reduce power consumption, by a factor of 10 and more, redesigning this specific function.

Table 2.1. Benchmark of Multi-frequency Sources

Publications	Tech.	Freq. (GHz)	Power ripple (dB)	PhN (dBc/Hz)	P_{DC} (mW)	Area (mm^2)
[A. Li, RFIC 2012] [1.1]	65nm CMOS	5.15 9.28	0.16	-129.94** -127.68**	1.92	0.23*
[S.-L. Jang, Microelectron Reliab. 2018] [1.2]	0.18µm SiGe	2.36 6.46	3.54	-115.88*** -101.01***	5.88	0.87
LETI [1.3-1.4]	**45nm CMOS SOI**	**2 2.5 3 3.5 4 4.5**	**2.4**	**-110.02*** **-111.77*** **-108.65*** **-106.86*** **-112.19*** **-109.78***	**84.4**	**0.27***

References for Table 2.1:

[1.1] A. Li and al., "A reconfigurable 4.7-6.6GHz and 8.5-10.7GHz concurrent and dual-band oscillator in 65nm CMOS," in 2012 IEEE Radio Frequency Integrated Circuits Symposium, Montreal, QC, Canada, 2012, p. 523-526.
[1.2] S.-L. Jang and al., "Dual-resonance concurrent oscillator," Microelectron. Reliab., vol. 83, p. 208-215, 2018.
[1.3] PhD Thesis: "Multi-tone frequency synthesis design and multi-qubits reflectometry readout modeling" by Mathilde Ouvrier-Buffet. theses.fr – Mathilde Ouvrier-buffet, Conception d'une synthèse de fréquence multi-tons et modélisation d'une lecture multi-qubits par réflectométrie.
[1.4] M. Ouvrier-Buffet & all, "Multi- Tone Frequency Generator for Gate-Based Readout of Spin Qubits", 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC).

2.2 Wideband D-Band RF Switches (ST 4.1.2)

CTA and ULUND have jointly investigated wideband D-band SPDT switches, across their design environments. Table 2.2 benchmarked technologies of primarily λ/4-shunt SPDT switches for D-band. Different technologies with similar topologies are compared to understand state of the art performance for D-band switches. Wideband D-band switches are a necessity in different kind of high frequency systems such as communication systems, radars, and remote sensing. The technologies that are considered within the SEQUENCE project are promising for usage within these applications.

Table 2.2. Benchmark of SPDT switches.

Ref.	Technology	Topology	First author affiliation	f_T/f_{MAX} (GHz)	Freq. (GHz)	Insertion loss(dB)	Isolation (dB)	r_{on}·C_{off} (fs)	Comment
[2.1]	32nm CMOS SOI	λ/4-shunt	Georgia Tech., USA (2015)	210/ 245	110-170	2.6-4	22	-	
[2.2]	50nm InGaAs mHEMT	λ/4-shunt	Fraunhofer IAF, Germany, (2018)	375/ 670	52-168	3.1	42.1	110.3	
[2.2]	50nm InGaAs mHEMT	Novel λ/4-shunt	Fraunhofer IAF, Germany (2018)	375/ 670	75-170	4.5	56.4	110.3	Impedance transform
[2.3]	0.13 um SiGe HBT	λ/4-shunt	Georgia Tech., USA (2014)	300/ 500	96-163	2.6-3	23.5-29	83.7	
[2.4]	0.13 um SiGe HBT	λ/4-shunt	IHP, Germany (2019)	300/ 500	110-170	2.0-3.0	21-26	-	
[2.5]	800 nm InP DHBT	λ/4-shunt	Ferdinand-Braun, Germany (2019)	350/ 350	90-170	3.0-5.0	42-55	-	

[2.6]	65 nm CMOS	λ/4-shunt	U.Toronto, Canada (2009)	300/ 400	110-170	4.0-5.0	26.5-32	-	
[2.7]	0.13 µm SiGe BiCMOS	RF MEMS	IHP, Germany (2017)	505/ 720	110-170	1.42-1.9	20-54.5	-	
CTA	50nm InGaAs NW	λ/4-shunt	C2Amps, Sweden (2021)	280/ 340	110-170	2.7	>20	135	Simulation
ULUND	50 nm InGaAs NW	λ/4-shunt	Lund U., Sweden (2023)	308/ 305	92-183	2.8	25.1	147	Simulation

State of the art performance is around 2-2.5 dB insertion loss and around 25 dB isolation for the standard λ/4-shunt topology, novel topologies can reach isolation up to 55 dB. The reported values for vertical nanowire switches are simulated results only, however the results show great promise especially considering the Ft/Fmax of the technology. There is great reason to look further into using the nanowire technology for high frequency band switches.

References for Table 2.2:

[2.1] W. T. Khan *et al*., "A D-band (110 to 170 GHz) SPDT switch in 32 nm CMOS SOI," *2015 IEEE MTT-S International Microwave Symposium*, 2015, pp. 1-3, doi: 10.1109/MWSYM.2015.7167061.
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[2.3] A. Ç. Ulusoy *et al*., "A Low-Loss and High Isolation D-Band SPDT Switch Utilizing Deep-Saturated SiGe HBTs," in *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 6, pp. 400-402, June 2014, doi: 10.1109/LMWC.2014.2313529.
[2.] A. Karakuzulu, A. Malignaggi and D. Kissinger, "Low Insertion Loss D-band SPDT Switches Using Reverse and Forward Saturated SiGe HBTs," *2019 IEEE Radio and Wireless Symposium (RWS)*, 2019, pp. 1-3, doi: 10.1109/RWS.2019.8714362.
[2.5] T. Shivan *et al*., "Highly linear 90-170 GHz SPDT Switch with High Isolation for Fully Integrated InP Transceivers," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 1011-1014, doi: 10.1109/MWSYM.2019.8700974.
[2.6] E. Laskin *et al*., "Nanoscale CMOS Transceiver Design in the 90–170-GHz Range," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3477-3490, Dec. 2009, doi: 10.1109/TMTT.2009.2034071.
[2.7] S. Tolunay Wipf, A. Göritz, M. Wietstruck, C. Wipf, and M. Kaynak, "BiCMOS embedded RF-MEMS technologies," *MikroSystemTechnik Kongress 2017 "MEMS, Mikroelektron. Syst. Proc.*, pp. 109–111, 2017.

2.3 Integration of LNAs and RF Switches (ST 4.1.3)

The D-band LNA benchmark is provided in Table 2.3. In general, for an LNA, regardless of carrier frequency, the most important performance metrics are the noise figure (NF), gain, linearity, and compression point. For validation of millimeter wave LNAs, there is often only one signal generator available, therefore, intermodulation measurements are often missing. A large bandwidth is desirable, since it makes the LNA more resilient to process spread. A high gain can be achieved by cascading several stages, at the prize of increased power consumption. The noise figure is to a large extent impacted by the fT/fMAX of the process technology. If the carrier frequency is too close to the cut-off frequency, the NF will deteriorate strongly. However, the back end of line (BEOL) of the process technology also has a significant impact, due to the limited Q-value of inductors and transformers. When comparing different LNAs it is important to distinguish between wafer and packages measurements. A commercial standalone LNA always includes a package that can add around 1 dB

loss at D-band frequencies. In Table 2.3, GaAs mHEMT, CMOS, GaN, InP DHBT, InP HEMT, SiGe, and Vertical Nanowire (VNW) designs are compared. For the InP HEMT, GaN DHFET and VNW designs, only simulated data is reported.

Table 2.3. Benchmark of D-band LNAs.

Ref.	Technology	Topology	Affiliation (Year)	f_t/f_{MAX} (GHz)	G_{pk} (dB)	BW (GHz)	Min NF (dB)	VCC (V)	P_{DC} (mW)	Comment
[2.8]	GaAs 40 nm mHEMT	4 stages	U. Rome, Italy (2017)	400/ 600	>20	115-160	4.0 @ 140 GHz	1.2	82	OMMIC foundry in France
[2.9]	GaInAs mHEMT 50 nm	3x Casc	Fraunhofer IAF, Germany (2017)	380/ 670	30.8	97-155	3.0 dB @ 119 GHz 3.4 (mean)	1.4	57.6	
[2.10]	CMOS 65 nm	SE, 2x CS	KAIST, Korea (2021)	-/ 310	17.9	11	4.7 @148 GHz, 6.2 @150 GHz	0.65	13.73	Advanced matching, narrowband
[2.11]	GaN DHFET T-gate 40 nm	6x SE	HRL, Malibu, USA (2017)	200/ 400	>25	110-170	~6 (projected)	5	225	NF not measured
[2.12]	InP DHBT	Single device	Brandenburg U. (2020)	330/ 350	-	-	6.0 @105 GHz	1.5	7.5	Device, W-band, wafer
[2.13]	InP HEMT	5x CS	Hangzhou Dianzi U., China (2018)	-/ -	>18.5	120-150	<4.5	-	47	Simulation only, wafer
[2.14]	SiGe 0.13 µm BiCMOS	CS, 2x Casc, CS	Sabanci U., Turkey, IHP (2018)	300/ 500	25.3	112-156	5.9 (fitted)	1.5/2.5	30	Wafer
[2.15]	SiGe 0.13 µm BiCMOS	2x Casc	Georgia Tech., USA (2015)	300/ 500	>20	110-140	5.5	2.0	112	Inductive CB base termination
[2.16]	SiGe 0.13 µm BiCMOS	4x Casc	Sabanci U., Turkey, IHP (2018)	300/ 500	32.6	52	4.8	-	28	NF <6.1dB across D-band
[2.17]	InP HBT 250nm	3x CE	IMEC (2022)	360/ 600	13	120-140	4-6	1.1	11.22	
CTA	50 nm InGaAs NW	Diff, 2x Casc	C2Amps (2022)	280/ 340	12	17	4.6	1.5	27.75	Simulated values

References for Table 3.2:

[2.8] R. Cleriti et al., "D-band LNA using a 40-nm GaAs mHEMT technology," 2017 12th European Microwave Integrated Circuits Conference (EuMIC), 2017, pp. 105-108, doi: 10.23919/EuMIC.2017.8230671.
[2.9] R. Weber, H. Massler and A. Leuther, "D-band low-noise amplifier MMIC with 50 % bandwidth and 3.0 dB noise figure in 100 nm and 50 nm mHEMT technology," 2017 IEEE MTT-S International Microwave Symposium (IMS), 2017, pp. 756-759, doi: 10.1109/MWSYM.2017.8058686.
[2.10] B. Yun, D. -W. Park, H. U. Mahmood, D. Kim and S. -G. Lee, "A D-Band High-Gain and Low-Power LNA in 65-nm CMOS by Adopting Simultaneous Noise- and Input-Matched Gmax-Core," in IEEE Transactions on Microwave Theory and Techniques, doi: 10.1109/TMTT.2021.3066972.
[2.11] A. Kurdoghlian et al., "First demonstration of broadband W-band and D-band GaN MMICs for next generation communication systems," 2017 IEEE MTT-S International Microwave Symposium (IMS), 2017, pp. 1126-1128, doi: 10.1109/MWSYM.2017.8058796.
[2.12] E. Kaule, R. Doerner, N. Weimann and M. Rudolph, "Modeling the Noise of Transferred-Substrate InP DHBTs at Highest Frequencies," 2020 German Microwave Conference (GeMiC), 2020, pp. 52-55.
[2.13] D. Yang, J. Wen, M. He and R. He, "A D-band Monolithic Low Noise Amplifier on InP HEMT Technology," 2018 12th International Symposium on Antennas, Propagation and EM Theory (ISAPE), 2018, pp. 1-4, doi: 10.1109/ISAPE.2018.8634087.
[2.14] B. Ustundag, E. Turkmen, B. Cetindogan, A. Guner, M. Kaynak and Y. Gurbuz, "Low-Noise Amplifiers for W-Band and D-Band Passive Imaging Systems in SiGe BiCMOS Technology," 2018 Asia-Pacific Microwave Conference (APMC), 2018, pp. 651-653, doi: 10.23919/APMC.2018.8617582.

[2.15] A. Ç. Ulusoy et al., "A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique," in IEEE Microwave and Wireless Components Letters, vol. 25, no. 1, pp. 61-63, Jan. 2015, doi: 10.1109/LMWC.2014.2369992.
[2.16] E. Turkmen, A. Burak, A. Guner, I. Kalyoncu, M. Kaynak and Y. Gurbuz, "A SiGe HBT D -Band LNA With Butterworth Response and Noise Reduction Technique," in IEEE Microwave and Wireless Components Letters, vol. 28, no. 6, pp. 524-526, June 2018, doi: 10.1109/LMWC.2018.2831450.
[2.17] V. Chauhan, N. Collaert and P. Wambacq, "A 120–140-GHz LNA in 250-nm InP HBT," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 11, pp. 1315-1318, Nov. 2022, doi: 10.1109/LMWC.2022.3189607.

3 Wireless Space Communication and Sensing at 40 – 70 K

3.1 Quadrature LO signals for the RX and TX chains (ST 4.2.1)

The direct-conversion transceiver architecture with zero-IF does not require any external filter. This means high integration level and low cost. However, the LO frequency is equal to the center frequency of the RF signal. This could result in issues with self-mixing in the receiver as well as LO pulling at the transmitter. A subharmonic mixer (SHM) typically utilizes the second-order harmonic of the mixer, thereby solving the issues above.

LO signal architectures-sub-harmonic generation

A subharmonic mixer [3.1-8] often uses the second order nonlinearity (2x SHM) of the mixer core. However, 3x SHMs [3.1] and 4xSHMs have also been designed. The mixing element could also be a Schottky diode. Yet another alternative is to create a LO signal that is rich in second order harmonics (LO signal with 25% duty cycle) [3.4]. This is however not really an alternative at mm-wave frequencies. A benchmark of sub-harmonic mixers is provided in Table 3.1. The diode-based SHMs usually have quite low gain, increasing the requirements on the preceding LNA. The SHMs based on active mixers have higher gain. An advantage is that the frequency of the VCO is reduced, thereby improving the phase noise. The referenced works do not have a PLL included.

Table 3.1. Sub-harmonic LO generation benchmark.

Ref.	Technology	Topology	PLL	Affiliation (Year)	f_T/f_{MAX} (GHz)	Max G_{conv} (dB)	freq. (GHz)	OP_{1dB} (dBm)	Isol. 2LO-RF (dB)	P_{DC} (mW)	Comment
[3.2]	0.13 µm SiGe BiCMOS	2xSHM, active mixer	No	MC2, Chalmers (2017)	250/ 370	2.6	98-140	-6	45	46	Switching core fund. tone, tail LO doubling
[3.3]	Skyworks Schottky diodes (DMK2308)	4xSHM, diode	No	Lahore, Pakistan (2015)	-	-13.4	57-59	-	>50	N/A	Discrete diode, simulation
[3.5]	GaAs 70nm mHEMT	2x SHM, Coupler, diode	No	Hangzhou, China (2020)	-	-16.2	110-170	-	In the meas. Noise floor	13.73	Broadband
[3.6]	CMOS 90 nm	2x SHM, active mixer	No	Taiwan U. (2018)	-	9	70-88	-	>40	5	High conversion gain, low PDC
[3.7]	0.13 µm pHEMT	2x SHM, diode	No	Plextek, UK (2012)	-	-11	71-86	-	-	-	-
[3.8]	CMOS 65nm	2xSHM, mixer	No	KAIST, Korea (2015)	-	3.4	75-81	-15.6	38	12	Gm-boost

References for (this section and) Table 3.1:

[3.1] H. Lee, J. Myeong and B. Min, "A 26GHz CMOS 3× Subharmonic Mixer With a Fundamental Frequency Rejection Technique," in *IEEE Access, vol. 8, pp. 122986-122996, 2020*, doi: 10.1109/ACCESS.2020.3007316.
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[3.4] Ali. M. Niknejad, "Advanced Mixers", 2014, http://rfic.eecs.berkeley.edu/ee242/pdf/Module_5_4_AdvMixer.pdf
[3.5] Shengzhou Zhang 3 and Lingling Sun 2 , "A Compact Broadband Monolithic Sub-Harmonic Mixer Using Multi-Line Coupler," *MDPI*, 2020.
[3.6] Y.-C. Wu, and H. Wang, "An E-band Double-Balanced Subharmonic Mixer with High Conversion Gain and Low Power in 90-nm CMOS Process," *IEEE microwave and wireless component letters,* vol. 28, no. 1, 2018.
[3.7] A. Dearn, L. Devlin and J. Nelson, "A sub-harmonic E-band IRM/SSB realized on a low cost PHEMT process," *2012 7th European Microwave Integrated Circuit Conference*, 2012, pp. 282-284.
[3.8] J. Jang, J. Oh and S. Hong, "A 79 GHz gm-boosted sub-harmonic mixer with high conversion gain in 65nm CMOS," 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2015, pp. 11-14, doi: 10.1109/RFIC.2015.7337692.

LO signal architectures-harmonic generation (no sub. harm. Mixer)

An LO architecture based on harmonic signal generation [3.9-14] is based around a VCO (or QVCO) that is at a fraction of the wanted carrier frequency. The upconversion to carrier LO frequency is not based on for instance the second order nonlinearity of the mixer core as for the sub-harmonic mixer, and the conversion gain is therefore higher. CTA has designed a circuit in this architecture and a benchmark of harmonic LO generation is provided in Table 3.2. For frequency multiplication, techniques such as injection locking, harmonic tripler circuits and upconversion active mixers can be used. The architectures are generally less complex than the ones used in the SHMs. Generally, at mm-wave frequencies, architectures that are based on polyphase filters for creation of different LO phases should be avoided, since the matching and process spread becomes worse with increasing frequency. Phase mismatch is also an issue for the QVCO in the selected topology. A competitive PLL should typically have a phase noise that is less than -90 dBc/Hz @ 1 MHz offset. The actual system requirement depends on the modulation scheme and the application. Typically, fixed radio links do not change their carrier frequency so PLL locking time is less of an issue. The PLL bandwidth can therefore be set low, which suppresses the phase noise of the VCO inside the loop bandwidth.

Table 3.2. Harmonic LO generation benchmark.

Ref	Technology	Topology	PLL	Affiliation (Year)	f_T/f_{MAX} (GHz)	PN (dBc/Hz@ 1MHz offset)	freq. (GHz)	P_{DC} (mW)	Comment
[3.9]	SiGe 0.18 µm BiCMOS	30 GHz PLL, tripler	Yes	UCLA, USA (2012)	200/ 180	-93 @96 GHz	90.9-101.4	140	Freq. tripler
[3.10]	CMOS 65 nm	Inj. Locked QVCO (QILO), tripler	Yes	Tokyo Tech. (2011)	-	-95 @60 GHz	58-63	80	20 GHz PLL, QILO freq. tripler
[3.11]	IBM CMOS 130 nm	Triple push VCO	No	Rensselaer Polytech., USA (2010)	-	-95 @ 10 MHz offset	55-65	95	Three VCO's @ 20 GHz
[3.12]	CMOS 65 nm	Doubler, IQ div.	Yes	Hong Kong U. (2015)	-	-92	59-86	54	Inj. locked freq. tripler

[3.13]	SiGe 0.18 µm	Sliding IF	No	Lund U. (2016)	200/ 250	-97.5 (est.)	81-86	109	Including QVCO and upconverter
[3.14]	SiGe 0.18 µm	28 GHz QVCO, active loop filter	Yes, no LO at carrier freq.	Lund U. (2016)	200/ 250	-107 @28 GHz	28	56.7	PN = -97.5 dBc/Hz @84 GHz
CTA	50 nm InGaAs NW	Sliding IF (as in 3.13 and 3.14)	No	C2Amps (2022)	190/ 280	-94 @ 28 GHz	28.0-30.4	77	PN= -84.5 dBc/Hz @1MHz offset at RT after upconversion to 84 GHz

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Conclusions LO generation in RT

Several options are available for LO generation for E-band mixers. However, the LO generation cannot be analyzed standalone. Instead, the performance of e.g. the mixer also sets the requirements on the surrounding blocks like the RX LNA. If there is significant attenuation in the mixer, the LNA will need to provide more gain to overcome the noise of the mixer.

It is advantageous to base the LO generation on a VCO that operates on a fraction of the LO-frequency since this improves the phase noise and reduces the power consumption of the VCO.

At mm-wave frequencies, the effect of capacitance mismatch becomes more severe, and it is difficult to control the phase of LO signal with accuracy. Architectures based on cancellation of unwanted harmonics by adding LO signals with different phases in subharmonic mixers are therefore less suitable. The use of polyphase filters for generating the required LO phases for subharmonic mixers cannot be recommended unless mismatch can be controlled.

A SHM always has lower gain for the harmonics than the fundamental. A passive SHM can be designed using anti-parallel Schottky diodes. These can be used in e.g. 2x or 4x SHM:s. It is a simple design, but a large drawback is the low conversion gain, often lower than -10 dB.

A low complexity of the LO generation is always desired. If the layout becomes complicated and matching is crucial, it is less probable to be successful without several iterations. **The selected**

topology for E-band LO generation is the sliding IF architecture based on a VCO that is the LO-frequency divided by three.

Compared to the SHM presented in [3.1], the VCO frequency could be selected to be the same as in the selected topology. In the sliding IF-architecture, the design is based on a QVCO, which is a slightly more complex topology. However, the active mixers in the selected topology operate on their fundamental LO frequency, thereby generating a substantial gain. With $f_{QVCO}= f_{LO}/3$ there is significantly less pulling of the VCO from PA in a transmitter.

A drawback is the more complex layout since both the four fundamental signals at 28 GHz and the second harmonic at 56 GHz need to be routed out from the QVCO without interfering with each other. A second drawback is the power consumption of the driver buffers for the 28 and 56 GHz LO signals. This topology, however, does not depend on cancellation of unwanted harmonics created in the SHM in [3.1], what is a large advantage.

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[3.1] H. Lee, J. Myeong and B. Min, "A 26GHz CMOS 3× Subharmonic Mixer With a Fundamental Frequency Rejection Technique," in *IEEE Access, vol. 8, pp. 122986-122996, 2020*, doi: 10.1109/ACCESS.2020.3007316.

3.2 E-Band RF Switches - Technology Level Sensitivity Analysis (ST 4.2.3)

ULUND have proposed to use a similar approach in the E-band as compared to the wideband D-band SPDT switch. Although the dual uplink-downlink specification (71 GHz-76 GHz, 81 GHz-86 GHz) yields an added design consideration, and this band is more accessible for standard technologies, it does not yield any unique benchmark compared to that presented for D-band circuits above. Instead, through collaboration between ULUND and CTA, the scaling implications and sensitivity of the III-V NW MOSFET technology in key parameters are investigated. Although on-resistance and off-capacitance are the most critical parameters for switch design, a special focus is here placed upon the interrelated device metrics and gain cut-off frequencies. The most important resistive and capacitive contributions are thereby collated. The study in this section is based on CTAs technology library.

Compact model parameter analysis of vertical III-V nanowire MOSFET technology

The compact model for the InGaAs vertical nanowire transistors used by CTA have been improved through iterative updates and new input during the SEQUENCE project. One key issue for modelling these scaled devices is the failure of traditional thermal noise models [3.15]. This was addressed in the model by the implementation of an updated suppressed shot-noise model that is adapted for quasi-ballistic devices [3.16, 3. 17]. In the continued overhaul of the compact model both self-heating effects [3.18] and trap-dynamic effects [3.19-20] have been introduced, what provides critical support for dynamic these effects. Last, but not least, interpolation between unpublished data shared by ULUND, on the DC-behaviour observed in cryogenic DC-measurements (15 K-300 K), has been used to model a continuous operation temperature dependence in the CTA model implementation.

Low frequency noise modelling was also propelled in SEQUENCE by a study that compare RT and cryogenic conditions for the vertical III-V nanowire MOSFET technology [3.21]. This analysis revealed that the main mechanism of 1/f-noise in these devices changes from carrier number fluctuations at RT (300 K) to carrier mobility fluctuations at cryogenic conditions (15 K), what is attributed to freeze-out of interface and border traps. Finally, for completeness in the following study, it is critical that a channel heterostructure and a field-plate on the drain side of the gate is used to engineer the

breakdown behaviour of the vertical III-V nanowire MOSFET [3. 22]. Grading to a higher bandgap in the high-field drain region, and simultaneous use of a field plate to lower the peak field, achieves a unique capability to operate a device with In-rich source at higher voltage. This performance boost is drawn from a suppression of band-to-band (BTB) tunnelling in the high-field drain region is also captured in the compact model.

To explore and identify which metrics of the devices that needs to be optimized to further improve the device technology for high-speed performance, a sensitivity study on several parameters in the compact model was performed. In short, 15 model parameters were selected and then the impact on performance metrics when scaling each parameter was investigated. In complement to the parametric sweep of on-resistance and off-capacitance already presented in SEQUENCE D4.4, this study provides a general view of the technology model and its capability in circuit design, even beyond RF-switches. The model parameters and nominal values for the transistor in this investigation are as follows:

Parameter	Nominal value [sweep range]	Description
*NW/NF**	50 [26, 110] unitless	Number of nanowires (in hex double row) per gate finger
*NF**	6 [2, 11] unitless	Number of gate fingers of the device
L	25 [10, 50] nm	Gate (channel) length,
d	25 [10, L] nm	Channel diameter, capped w.r.t. gate length
V_{bd}**	0.6 [0.75, 1.0] V	Breakdown voltage (sweep only valid for C_{gd2} case)
R_d	170 [85, 340] ohm µm	Drain resistance
R_s	70 [29, 117] ohm µm	Source resistance
R_g	0.056 [0.028, 0.084] ohm m	Gate resistance
C_{gs}	0.31 [0.15, 0.62] aF/wire	Input (gate-source) capacitance
C_{gse}	6.0 [3.0, 12] fF	Input (gate-source) capacitance, extrinsic
C_{gde}	0.99 [0.50, 1.98] fF	Feedback (drain-gate) capacitance, extrinsic
C_{sd}	4.6 [2.3, 9.2] fF	Output (drain-source) capacitance
C_{gd1}	0.046 [0.023, 0.092] aF/wire	Feedback (drain-gate) capacitance 1, without field plate
C_{gd2}	0.039 [0.012, 0.078] aF/wire	Feedback (drain-gate) capacitance 2, with field plate
C_{inv}	7.9 [3.9, 16] fF/µm^2	Inversion charge capacitance, oxide and semiconductor
T	0.58 [0.29, 0.88] unitless	Channel ballisticity factor
mu, aka μ_{eff}	1220 [610, 1830] cm^2/Vs	Effective channel mobility

*not used as an independent sweep variable in this study, **affected by use and length of field plate

The investigated device geometry used a fixed total number of nanowires, NW = 300, distributed over fixed number of fingers, NF = 6. The nominal gate length, L_g = 25 nm, and wire diameter, d = 25nm, in this numerical study were selected to represent a relatively scaled device. Each of the parameters were swept in 10 steps and for each step the gate-source voltage, V_{GS}, was swept in 20 steps, yielding an overall drain current, I_D, range from 18 µA per wire up to 87 µA per wire (5.3-26.1 mA). The drain-source voltage, V_{DS}, was held constant at 0.6 V. The performance metrics analysed in this study were the DC transconductance per gate width, $g_{m\_DC} = g_m/W$, the current gain transition frequency, f_T, and the maximum oscillation frequency, f_{max}. Note that this was done in sequence for each parameter, with all other parameters held at the nominal value. The bias optimisation goal was peak f_T and f_{max}, identified per –20 dB/dec gain extrapolation beyond the first-order corner. It was found for all device parameter variations that both f_T and f_{max} were maximised at the same bias point. For the nominal setting, the vertical III-V MOSFET achieves g_{m_DC} = 2.68 mS/µm, f_T = 273 GHz, and f_{max} = 384 GHz.

High-speed technology performance must be based on excellent DC characteristics. The DC transconductance, g_{m_DC}, is a key parameter, deeply interrelated with the gain capability and on-resistance of the nanowire MOSFET. The transconductance sensitivity from each model parameter is shown in Fig. 3.1, what is presented in mS/µm per percentage model parameter change.

The largest positive impact on transconductance is found for the inversion layer capacitance, C_{inv} comprising the series combination of the gate oxide and semiconductor capacitances, and the ballisticity factor, T, governing the balance between ballistic and diffusive transport characteristics

through the channel. Both of these parameters relate directly to the number of charges in transport, *i. e.*, the drive current level. Under electrostatic control, this contributes directly to transconductance.

The largest negative impact on transconductance is found for channel length, L, and the channel diameter, d, closely followed by the breakdown voltage, V_{bd}. Channel length scaling is both related to increased channel resistance in the diffusive limit ($T \rightarrow 0$) and inversely related to ballisticity in the ballistic limit ($T \rightarrow 1$). Channel diameter scaling is related to loss of electrostatic control and the effect seen here is combined with that of normalisation over a larger circumference. Source and drain resistances, R_s and R_d, respectively, are also responsible for transconductance degradation. The source resistance in particular since it provides degenerative feedback whereas the drain resistance merely loads the device. It is critical to reduce these access resistances.

To improve transconductance, g_{m_DC}, the largest impact will come from optimizing the electrostatics of the transistor, in combination with improving the transport conditions inside the channel and its access regions. Gate length scaling is also important to push the limits of the technology. This can only be done to the limit of saturating increased transconductance and ballisticity in balance to the negative impact of increased output conductance, what is again limited by transport and electrostatics. This analysis can guide further experimental investigations.

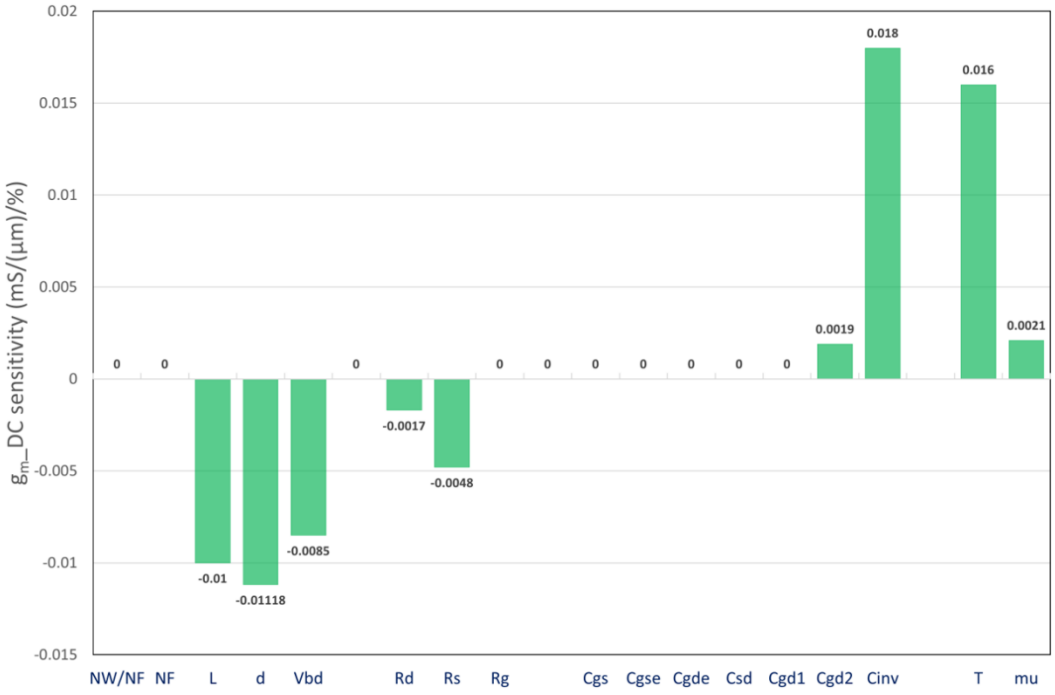

Figure 3.1: Nominal DC transconductance sensitivity to percent model parameter change.

A more holistic view on the circuit level capabilities of a technology can be seen from the perspective of gain cut-off frequencies. In Fig. 3.2, the sensitivity of f_T and f_{max} for the same model parameter perturbations is shown. Again, it is found in this perspective that inversion capacitance, C_{inv}, and ballisticity, T, play an important role, but also the gate drain capacitance can be identified as the most important model parameter to improve f_T and f_{max}. Among the parasitic resistances, the drain resistance, R_d, has the largest impact. This shows the importance of not only optimising single device DC metrics, such as DC transconductance, in the pursuit of high-speed performance in a device technology. The core DC performance gives a baseline but must be complemented by a low-loss and low-capacitance interconnect environment to provide potential for competitive circuit design.

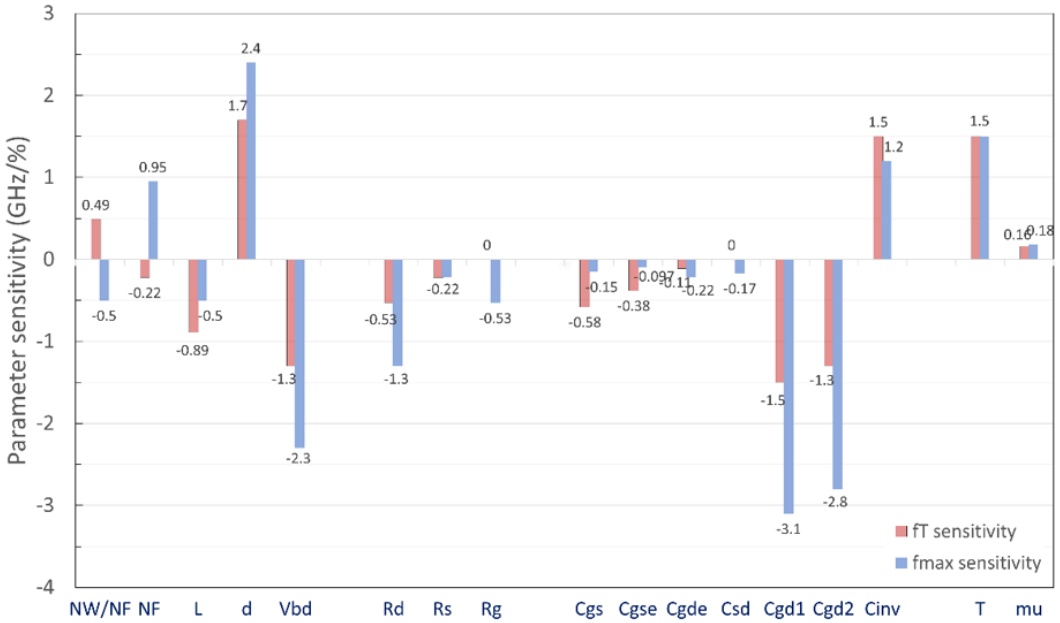

Figure 3.2: Nominal f_T and f_{max} sensitivity in GHz per percent model parameter change.

The next step in the sensitivity analysis is to further explore the effect on f_T and f_{max} for parametric sweeps of a selection of model parameters. The selected parameters are gate-drain capacitance, C_{gd1}, drain resistance, R_d, and channel diameter, d, see Fig. 3.3-5, respectively. These results provide additional information on the scaling behaviour for the selected parameters and are commented in the following. Although other parameters, such as breakdown voltage, V_{bd}, channel ballisticity, T, and inversion capacitance, C_{inv}, clearly contribute to the performance, these parameters are indirect results of complex geometry and quantum-confined short-channel device physics. Such indirect parameters are key for the device performance but not possible to directly and independently address with specific device process changes. The fabrication trade-offs are subject to ongoing research.

The gain cut-off dependence on gate-drain feedback capacitance (without field plate), C_{gd1}, is shown in Fig. 3.3. The gate-drain capacitance can be affected by electrode overlap, but especially by the choice of dielectric environment and thickness (drain spacer engineering). There is a clear exponential decay in both gain bandwidths for increased feedback capacitance, but the strongest effect is seen in maximum oscillation frequency. Halving the value of C_{gd1} in the model indicates a potential for gain performance pushed from below f_{max} = 250 GHz to beyond f_{max} = 650 GHz; a very competitive value.

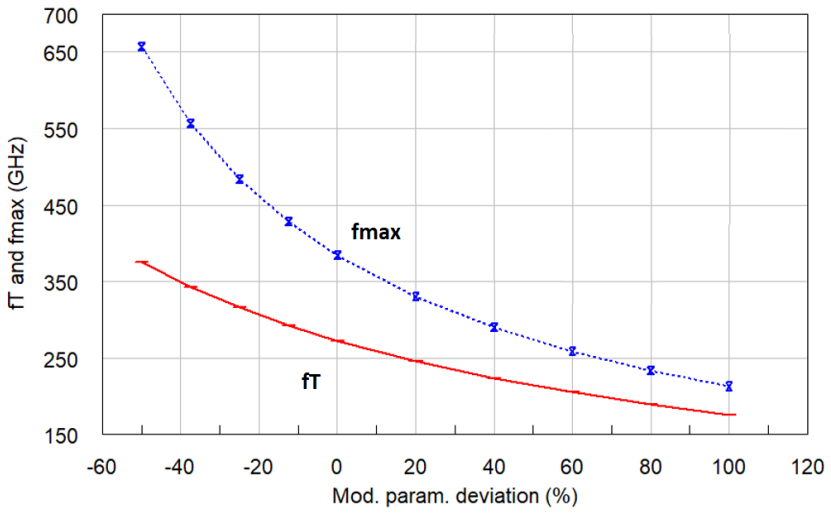

Figure 3.3: Current gain transition, f_T, (red) and maximum oscillation, f_{max}, (blue) frequency sensitivity with respect to relative changes in the feedback capacitance, C_{gd1}, model parameter.

The gain cut-off dependence on drain resistance, R_d, is shown in Fig. 3.4. Drain resistance can be affected by contact deposition procedures, including pre-cleaning, material choice, and post deposition annealing. It is seen that while maximum oscillation frequency shows an exponential decay, the effect on current gain bandwidth is rather a linear function with negative slope. Halving the value of R_d in the model indicates a potential for gain performance beyond f_{max} = 450 GHz. This adds further leverage to the effect of feedback capacitance reduction discussed in the paragraph above. Synergetic addition of these effects should be targeted, among all other performance considerations.

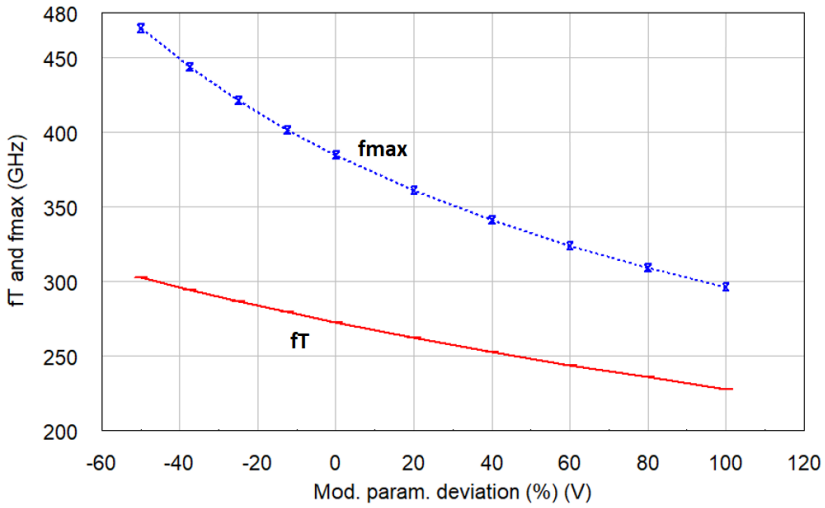

Figure 3.4: Current gain transition, f_T, (red) and maximum oscillation, f_{max}, (blue) frequency sensitivity with respect to relative changes in the drain resistance, R_d, model parameter.

The gain cut-off dependence on channel diameter, *d*, is shown in Fig. 3.5. Increased diameter, what can be affected by the pre-growth catalyst patterning, contributes both to more gate width and to wider access regions with less series resistance. There is nearly linear dependence on both gain bandwidths with respect to increased diameter. This is counter-intuitive in relation to the corresponding negative transconductance sensitivity, shown above, but is reasonable from the perspective of effective channel width per chip area. Note that the transconductance perspective suffers from misalignment of the peak performance due to gain bandwidth-focused bias optimisation. To generalise, densification of the vertical device structure provides a better balance between intrinsic performance and parasitic elements.

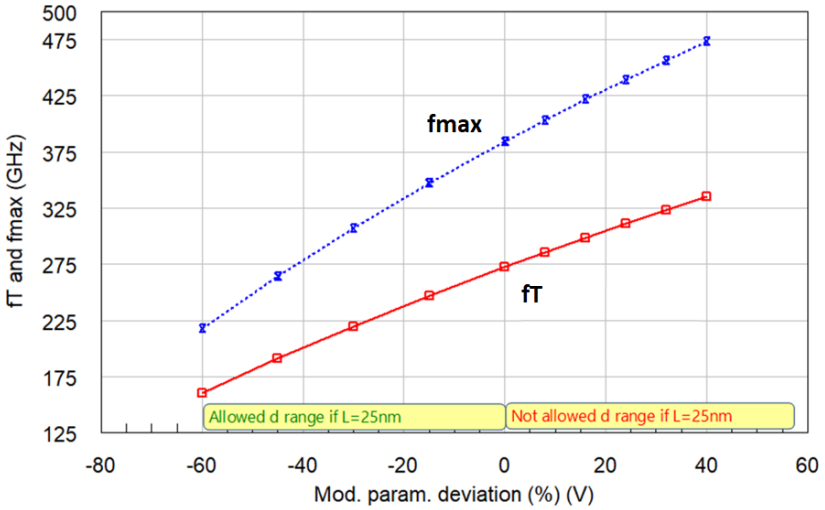

Figure 3.5: Current gain transition, f_T, (red) and maximum oscillation, f_{max}, (blue) frequency sensitivity with respect to relative changes in the channel diameter, d, model parameter.

To summarise, the analysis of the compact model parameters shows that to achieve improved performance in the vertical nanowire transistor technology, several parameters need to be considered. The most important parameter has been identified to be the gate-drain capacitance, C_{gd}, (indexed suffix indicating without or including field plate) but also the channel transport mechanism here collated as ballisticity, T, the electrostatics connected to inversion charge density, C_{inv}. This is also considered in the context of channel diameter, d, what is intertwined with and affects many aspects of the device. Furthermore, the series parasitic resistances have a significant impact on the device performance, where especially the drain resistance, R_d, is found to limit high-frequency gain.

This sensitivity analysis shows that high-speed performance in the vertical III-V nanowire MOSFET technology benefit from nanowire density increase. An increase in amount of channel width per chip area through diameter increase is explored here specifically. This is a partial result as a reduction of the nanowire pitch will be similarly beneficial, linked to increased amount of channel per area. Density scaling will thereby add drive current and transconductance in relation to an approximately fixed amount of parasitic capacitance. It is also important to note that the nanowire diameter will be intertwined with the achievable gate length definition. This will link to other key parameters, such as inversion capacitance and channel ballisticity, that are also shown to be important but require further experimental investigation. It is furthermore important, not surprisingly, to balance the minimisation of gate-drain feedback capacitance to the penalty of added drain resistance. The top spacer process is key in this aspect and will be a continued focus for device optimisation, together with the general interconnect and BEOL environment.

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3.3 E/W-Band LNAs and RF Switches (ST 4.2.3)

The E/W-band frequency range is interesting for a multitude of applications. Earth observation satellites use frequencies around 89 GHz in microwave imager systems for, e.g., rainfall detection. In such systems the noise figure is the most important parameters. Thus, a monolithic integration of the LNA and a switch, used as Dicke switch, is very attractive since the omission of assembly losses due to, e.g., bond wires between switch and LNA can improve the system noise performance considerably. Furthermore, the frequencies between 71 – 76 GHz and 81 – 86 GHz are investigated for satellite communication. Also, this application can benefit from a monolithic integration of the LNA and a switch. However, in open literature, results with a monolithic integration of LNA and switch are rarely reported in E/W-band. One of the rare examples was recently presented and is based on a GaN-on-SiC technology [3.23]. The receive path including switch and LNA achieve an average noise figure of 4.5 dB between 75 – 86 GHz. However, apart from this reference results are limited. Thus, the literature survey in this deliverable for E/W-band switches and LNAs is separated, considering the switch and LNA separately. Table 3.3 gives an overview about best SPDT switch results in various technologies and Table 3.4 compares LNAs.

Table 3.3. State-of-the-Art E/W-Band SPDT Switches.

Ref.	Technology	Topology	First author affiliation	f_T/f_{MAX} (GHz)	freq (GHz)	Insertion loss(dB)	Isolation (dB)	$r_{on} \cdot C_{off}$ (fs)	Comment
[3.24] Part of SEQUENCE	50nm InGaAs mHEMT	λ/4-shunt	Fraunhofer IAF, Germany, (2020)	375/ 670	50-75 75-110	1-1.6	>31.6 >28.5	84	
[3.25]	GaAs diode	λ/4-shunt	Fraunhofer IAF, Germany, (1999)	n/a	75-110	1.1-1.6	>31	75	
[3.26]	100 nm GaN HEMT	λ/4-shunt	Fraunhofer IAF, Germany, (2018)	n/a	72-131	1.1-2	>18.5	210	
[3.27]	150 nm GaAs pHEMT	λ/4-shunt	U. Seoul, Korea (2014)	n/a	40-85	1.2-2	>31	n/a	
[3.28]	SiGe diode	λ/4-shunt	Georgia Tech., USA (2014)	300/ 350	77-133	1.4-2	>19	n/a	

Table 3.4. State-of-the-Art E/W-Band LNAs.

Ref.	Technology	Topology	Affiliation (Year)	f_T/f_{MAX} (GHz)	Max S21 (dB)	BW (GHz)	NF (dB)	VCC (V)	P_{DC} (mW)	Comment
[3.29] Part of SEQUENCE	50 nm InGaAs mHEMT	4 stages CS	Fraunhofer IAF, Germany, (2023)	375/ 670	>28.5	75-110	1.5-2.0 (av 1.7)	0.6	25.5	
[3.30]	35 nm InGaAs mHEMT	4 stages CS	Fraunhofer IAF, Germany (2019)	515/ >1000	28	75-110	1.7-2.2 (av 1.9)	0.6	40.8	
[3.31] Part of SEQUENCE	20 nm InGaAs MOSHEMT	4 stages CS	Fraunhofer IAF, Germany (2020)	275/ 640	20	75-100	2.3-3.2 (av 2.8)	0.6	69.7	
[3.32]	70 nm GaN HEMT	4 stages CS	Fraunhofer IAF, Germany (2022)	145/ >300	24	63-101	2.8-3.3 (av 3)	5/7.5	307	
[3.33]	100 nm pHEMT	4 stages CS	UMS, France/Germany (2012)	130/ n/a	22.4	71-86	2.7-4.3	3.5	262.5	
[3.34] Part of SEQUENCE	35 nm InGaAs mHEMT	Distributed amplifier	Fraunhofer IAF, Germany (2019)	515/ >1000	13.6	75-110	3.5-5 (av 3.6)	0.8	346	dist. amp. covering a total BW from 1-330 GHz
[3.35]	22 nm Si FinFET	2 stages cascode	Intel, USA (2018)	n/a	20	67-79	3.7-4.5	1	10.8	
[3.36]	SiGe 0.13 µm BiCMOS	2 stages cascode	U. Southeast, China (2021)	200/ 250	21.3	72.5-84	4.5-5.5	2.5	52	

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4 Cryogenics Logic and Mixed Signal Circuits

4.1 III-V nanowire FET Digital Circuits (ULUND)

ULUND has presented current mode logic circuits in III-V nanowire TFET technology. In addition to the performance comparison presented elsewhere, we here quantify the energy delay product (EDP) in Table 4.1. This complements the power delay product (PDP), which is a design-level metric, with a technology-level metric, to enable better comparative understanding of the TFET technology offer. It is clear that the III-V nanowire TFET technology can offer operation at an extremely low power dissipation, < 100 pW per logic gate, but that this comes at the price of extremely slow operation, > 1 us per logic gate. The best tradeoff from an EDP perspective is fund at 26 uW per gate, using a

1 kohm resistive load. These breakthrough devices are still experimental and have yet to find an application where the CML operation paradigm can present a uniquely required performance offer.

Table 4.1: Simulated oscillation frequency of the 5-stage CML ring oscillator for different designs / bias points, targeting power dissipation limits of 1, 10, and 100 µW per logic gate (CML inverter stage). Also presented is the corresponding propagation delay and power dissipation per CML inverter stage, yielding power delay product and energy delay product metrics for benchmarking.

Load type	Bias (V)	Freq. (MHz)	Propag. delay (ns)	Power diss. (uW)	PDP (fJ)	EDP (fJ*ns)
Resistive (100 kΩ)	0.5	0.90	110	1.45	160	18000
Resistive (1 kΩ)	0.5	140	0.7	25.8	18	13
Resistive (100 kΩ)	0.3	0.23	440	0.83	365	161000
Resistive (1 kΩ)	0.3	25.0	4	7.75	31	124
Resistive (100 kΩ)	0.1	0.08	1300	0.06	78	101000
Diode conn. TFET	0.5	0.90	110	9.2	1012	111000
PMOS active load	0.5	8.4	12	0.4	5	58

These results provide a point of reference, but are not mature enough for comparative benchmarking.

4.2 FD-SOI CMOS Digital Circuits (LETI)

Last works in quantum computing show the need of mixed-signal ICs, capable of operating at extremely low temperatures (below 10 K), for qubits control and read-out. In such cryo-systems, oscillators are crucial blocks, for instance, in LO frequency generation in order to up/down convert baseband signals for the quantum processor. In the future, quantum computers should be able to calculate with millions of qubits, suggesting that the same number of microwave carriers should be required [4.16]. In this context, digital Ring-VCOs with multiple stages based on CMOS technologies could offer a much smaller overall area compared to classic analog LC-VCOs in order to generate such large numbers of carriers. That is why, in the framework of SEQUENCE Project, we have designed a High-Frequency RO tunable from 5 GHz to 15 GHz, made in 28-nm FD-SOI CMOS technology from STMicroelectronics.

Tables 4.2-3 compare performance of this Ring Oscillator with the State-Of-the-Art at Room Temperature and Cryogenic Temperature, respectively. You can note two types of topology CML or CMOS. CML Ring Oscillators are more used for III-V/SiGe technologies and present best phase noise at the expense of power dissipation whereas CMOS Ring Oscillators like this work exhibit better energy efficiency and integration. In comparison to other ROs, our cryo-RO present excellent gate propagation delays (between 5.1 ps and 7.1 ps) at RT (Room Temperature/300K). We hope that these values will be improved as we saw in simulation at CT (Cryogenic Temperature/4K).

Table 4.2. Benchmark of Ring Oscillators at RT (Room Temperature).

Ref.	Techno-logy	Topo-logy	Affiliation (Year)	f_T / f_{MAX} (GHz)	f_{osc} (GHz)	τ_p (ps)	P_{diss} (mW)	f_{min} / f_{max} (GHz)	N stag.	L@10MHz (dBc/Hz)	Comment
[4.1]	1.5 um InP HBT	CML	U. Toronto (2001)	100 / NA	18.6	34.5 / 22	130	14.5 / 22.7	1	-109.5	
[4.2]	0.12 um SOI CMOS	CML	IBM, Hopewell (2003)	150 / 230	29	6 / 5.4	22.5	27.5 / 30.5	3	-95.9	

[4.3]	0.18 um SiGe HBT	CML	Georgia Tech., USA (2005)	120 / NA	32	16.6 / 14.7	87	30.1 / 33.9	1	-103	
[4.4]	0.12 um SiGe HBT	CML	UCSD, USA (2006)	207 / 285	24.3	12.1 / 8.9	105.6	20.7 / 27.9	2	-105	
[4.5]	90 nm CMOS	CML	Cheng-Kung U., Taiwan ROC (2013)	150 / 200	16.5	16.7 / 13.9	8.7	15 / 18	2	-124.6	L extrapolated from 1MHz offset
[4.6]	0.5 GaN HEMT	CML	Chang Gung U. Taiwan ROC (2013)	12 / 20	5.74	43.8 / 43.4	900	5.71 / 5.76	2	-135	
[4.7]	0.13 um SiGe HBT	CML	Technion, Israel (2019)	250 / 340	38.5	7.2 / 5.9	132	34.7 / 42.2	2	-95	
[4.8]	0.13 um SiGe HBT	CML	TU Dresden, Germany (2021)	350 / 450	16.5	10.3 / 6.1	189	9.7 / 16.5	5	-106.3	@293K
					13	8.5 / 5.4	180	8.4 / 13.3	7	-107.3	
[4.9]	0.13 um SiGe HBT	CML	Georgia Tech., USA (2010)	240 / 330		2.73	248		53	NA	
[4.10]	45 nm PD-SOI CMOS	CMOS	Raytheon BBN, USA (2010)		0.618		0.55		100	NA	
[4.11]	Nanowi-re SOI CMOS	CMOS	CEA LETI, France (2016)		1.3				20	NA	
[4.12]	0.16-µm CMOS	CMOS	Delft UT, The Netherlands (2018)		2.5m	38.3		1.2m / 4.7m	2703	NA	
[4.13]	28 nm FD-SOI CMOS	CMOS	CEA LETI, France(2018)	250 / 250		27 / 14	0.08		101	NA	@296K Ultra Low Power
[4.14]	0.18µm CMOS	CMOS	U. Sci. Tech. Hefei, China, (2019)			64.8 /13.2	0.2		101	-155 / -153	Simulated results
This Work	III-V NW TFET	CML	Lund U., Sweden (2023)	- / -	0.14	0.7	0.03		5	NA	Simulation
This Work	28 nm FD-SOI CMOS	CMOS	CEA LETI, France (2023)	250 / 250	13.1/9.7/7.8/6.8	7.1 / 5.1	10*	6.4 / 19.5	5/7/9 /11	-80	@300K *with Output Buffer

Table 4.3. Benchmark of Ring Oscillators at CT (Cryogenic Temperature).

Ref.	Techno-logy	Topo-logy	Affiliation (Year)	f_T / f_{MAX} (GHz)	f_{osc} (GHz)	τ_p (ps)	P_{diss} (mW)	f_{min} / f_{max} (GHz)	N stag.	L@10MHz (dBc/Hz)	Comment
[4.8]	0.13 um SiGe HBT	CML	TU Dresden, Germany (2021)	350 / 450	18	6.6 / 5.6	189	15.2 / 18	5	-96	@6K
					13.5	8.1 / 5.3	180	8.8 / 13.5	7	-88	
[4.9]	0.13 um SiGe HBT	CML	Georgia Tech., USA (2010)	240 / 330		2.31	133		53	NA	@25K
[4.10]	45 nm PD-SOI CMOS	CMOS	Raytheon BBN, USA (2010)		0.742		0.57		100	NA	@2.8K
[4.11]	Nanowi-re SOI CMOS	CMOS	CEA LETI, France (2016)		1.5				20	NA	@4.2K

[4.12]	0.16-µm CMOS	CMOS	Delft UT, The Netherlands (2018)		3.5m	30.6		1m / 6m	2703	NA	@4K
[4.13]	28 nm FD-SOI CMOS	CMOS	CEA LETI, France (2018)	250 / 250	0.38	18 / 10	0.13		101	NA	@4.3K Ultra Low Power
[4.14]	0.18µm CMOS	CMOS	U. Sci. Tech. Hefei, China (2019)			179.2 / 76.7	0.6		101	-178 / -174	Simulated results
[4.15]	28 nm FD-SOI CMOS	CMOS	CEA IRIG, France (2020)	250 / 250	6.9		0.27	0.1 / 6.9	5	NA	@0.11K
This Work	28 nm FD-SOI CMOS	CMOS	CEA LETI, France (2023)	250 / 250				3 / 22	5/7/9 /11	-80	Simulated results

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5 Summary and conclusions

This deliverable reports on benchmarking of the circuit design results in SEQUENCE. The consortium has investigated a wide range of circuits for wireless wideband communication and sensing applications at room temperature and wireless space communication and sensing and 40-70 K as well as digital building blocks. The technologies developed are based on Si CMOS FD-SOI, III-V HEMTs and III-V nanowire MOSFETs. The benchmarking results demonstrate a broad capability to address contemporary challenges in monolithic circuit design that require cryogenic 3D nanoelectronics.

The benchmarking results presented here summarise the SEQUENCE contribution in circuits for wireless wideband communication and sensing applications at room temperature and wireless space communication and sensing and 40-70 K. as well as digital building blocks. This multifaceted pathfinding activity provides an updated baseline and will guide continued research in the field. Specific conclusions partners and their technologies are provided in the following.

LETI:

The FDSOI 28nm process from ST has been evaluated for cryogenic applications at 77°K for space applications, and around 4°K for Quantum computing, the two explorations in WP4 were digital like (Ring oscillator) and RF (LNA). In addition, an architecture for multi–RF sources (quantum computing), multi-LO (communication) has been validated in the 1-8 GHz bandwidth, the process used was GF45 RF SOI, as this circuit was designed to be used at room temperature, and signals can be sent to cryogenic temperature through RF guides.

FDSOI 28nm from ST is a very good compromise designing the readout control circuit for quantum computing around 4°K, the capability to modify the VT behaviour of the transistors through the back gate is a true added value, which allows optimising the circuit at 4°K and under. The fact that digital performances modifying the back gate voltage are similar than they are at ambient temperature opens the door to a digital RF transceiver approach, reducing the power consumption and thus the temperature increase close to the Qubit.

At temperature range between 30°K and 77°K, the FDSOI 28nm digital performances seem better than they are at ambient temperature which opens the door to optimised power efficient computing functions in this temperature range for high performance computing applications, and can increase the power efficiency of signal processing functions in satellite communication functions.

FDSOI 28nm has not best in class cryogenic LNA performances, presently this limits their use in the cryogenic applications as Quantum computing and space communication. Specific architecture must be explored, at least for Quantum computing to improve LNA performances. The main motivation is to integrate all the FDSOI Readout circuits with the FDSOI Qubits on the same die. Another low-cost alternative would be to explore SiGe HBT LNAs, in this case two dies must be placed in the cryostat, the FDSOI readout IC with Qubits, (except the LNA), and the SiGe HBT LNA. This SiGe LNA could address also Space applications.

Finally, the multi-LO multi-source architecture, answers to the QC request, and the communication request. This could be implemented in FDSOI for 4K readout applications, needing only one low frequency reference, or in SiGe HBT for High-speed communication.

These results, and the strong relationship LETI had with STMicroelectronics during this project, convince them to participate to the next step KDT ARCTIC project targeting technology platform for cryogenic applications, and Didier Belot left LETI to join ST to coordinate this effort on two technologies, FDSOI and BiCMOS55, (SiGe HBT plus 55nm CMOS process). ST's objective through this KDT project will be to adapt their process offer to cryogenic applications, to be present in the European Quantum Computing initiative, and to reenforce their position in civil satellite communications.

The second main outcome for LETI is the creation of SIQUANCE Start-Up which will address FDSOI SPIN Qubit Quantum Computing, and which will base their read-out circuits on FDSOI results obtained in SEQUENCE. In addition, SIQUANCE is partner of the KDT ARCTIC proposal with ST and LETI to accelerate the development of an industrial solution for FDSOI SPIN Quantum Computing.

We consider that the implication of ST in cryogenic applications, and the creation of SIQUANCE are the outstanding SEQUENCE outcomes for LETI, this obviously includes all partners, as ST was one of the industrials, we visited in our roadshow dissemination activity, and we invited a key ST process person, Pascal Chevalier, ST-Fellow, for the Winter-school we organised in 2022.

IAF:

III-V HEMTs with an InGaAs channel and Schottky gates clearly demonstrate the benchmark for RF noise figures over the entire millimeter-wave frequency range. Thus, LNAs realized in the used 50 nm InGaAs mHEMT technology achieve the lowest noise figure compared over a wide range of semiconductor technologies. LNAs in the 20 nm InGaAs MOSHEMT technology demonstrate promising first LNA results in the frequency range around 100 GHz. However, there is still a clear performance gap to dedicated low-noise technologies based on a Schottky gate. Apart from dedicated low-noise technologies, the competition for best noise figures is strong among all other technologies. Due to improvements of modern GaN HEMT technologies, the demonstrated noise figures are promising – in combination with an output power which is by a factor of approx. 10 higher. However, depending on the circuit topology also dedicated low-noise technologies can improve the linear power level by a factor of up to 10 with an only slightly degraded noise figure. This is a result of much higher cut-off frequencies of the dedicated low-noise technologies.

Also for RF switches in the E/W-band frequency range, the demonstrated results in the 50 nm InGaAs mHEMT technology achieve the best values in terms of insertion loss and isolation. When comparing different technologies, the demonstrated insertion loss values appear rather similar. The comparison of various technologies in terms of isolation shows a much stronger difference. Due to a low on-resistance, low-noise technologies, such as the used 50 nm InGaAs mHEMT technology, achieve a comparable isolation so that the combination of a lowest insertion loss and a high isolation result in a state-of-the-art switch performance.

The fact that the used 50 nm InGaAs mHEMT technology achieve for both topologies (LNAs and switches) a state-of-the-art performance, whereas other technologies exhibit only in one of the two categories (if at all) state-of-the-art performance, proves as well the benefit of a monolithic integration of switch and LNA in the used 50 nm mHEMT technology as it was demonstrated within SEQUENCE.

ULUND/CTA:

III-V nanowire MOSFETs are a clear candidate for high-frequency analogue circuit design, with a performance profile that complements the excellent low-noise high-speed HEMT technologies. The epitaxially grown vertical nanowire MOSFETs, on silicon substrates, uniquely bring a capability for bandgap engineering along the channel. This can, in combination with the inherent 3D connectivity, be beneficial in applications where high-speed performance must be combined with voltage handling. The remaining challenge is to demonstrate this device technology in larger scale circuits.

The nanowire benchmark presented here shows a competitive performance in SPDT switch applications, with further capabilities beyond. Harmonic signal generation is also proposed in this technology, highlighting the versatility of the devices. Our parametric investigations in relation to E-band implementations, based on predictive modelling, further highlight the interrelation between high-speed performance and switch-centric parameters. Key factors for improved high-speed capability in the vertical III-V nanowire technology, beyond the DC-centric transconductance and source resistance, respective, parameter maximization and minimization, are increased nanowire density and a focused trade-off between gate-drain feedback capacitance and drain resistance. This promises a capability to integrate key circuitry in the same III-V nanowire technology.