Deliverable – D4.2

Project acronym	SEQUENCE
Project number	871764
Project title	Cryogenic 3D Nanoelectronics (Sense and Readout Electronics Cryogenically Integrated for QUantum ENhanced Computation and Evolving Communication)

Document Properties	
Nature of Document	Report
Work Package	WP4 - Communication and Sensing
Task Leader	Beneficiary 1 – IAF
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Version	1.0
Status of Document	Draft
Due Date of deliverable	M18
Actual delivery date	M18
Dissemination Level	PU

Document history			
Version	Date	Author	Status – Reason for change
0.0	2020-12-16	Didier Belot	Initial Draft
0.1	2021-06-17	Simon Olson, Tobias Tired (CTA), Didier Belot (LETI), Antonio D'Amico (EPFL), Lars Ohlsson Fhager (ULUND), Fabian Thome (IAF)	Report
0.2	2021-06-18	Fabian Thome	Report

Release approval			
Version	Date	Name and organisation	Role
1.0	2021-06-24	Lars-Erik Wernersson	Project Coordinator

Disclaimer:

The project has received funding from the European Union's Horizon 2020 research and innovation programme under Grant agreement number 871764 (SEQUENCE)

Contents

Introduction

This deliverable summarizes the design activities of the SEQUENCE partners in work package 4. The deliverable highlights several techniques and results in the area of low-noise amplifiers (LNAs), switches, and signal generation in various frequency ranges and for different applications.

CTA is working on a sliding IF architecture for generating the quadrature LO signals at E-band frequencies. This architecture has been selected after careful evaluation of other possible topologies. We have chosen to target the band at 81 – 86 GHz and initially design the TX part. Work tasks involves design of a Quadrature Voltage Controlled Oscillator (QVCO) and upconversion mixers. CTA is also working on D-band switch and LNA circuit designs as well as identifying limiting factors in the vertical nanowire technology with regards to these blocks.

LETI is working on a multi-frequency generator for sub-20 GHz communication and spin Qubit manipulation implemented in an RFSOI process, and is evaluating the cryogenic digital potentiality of FDSOI through a Ring-Oscillator design.

IAF is working on an integrated solution of a single-pole double-throw (SPDT) switch and an LNA at W-band frequencies (75 – 110 GHz). The designs target satellite-sensing applications at operating temperatures of approximately 50 K.

Designing at very low temperature (<4 K) presents new challenges for the engineers and an accurate noise model is instrumental in this regard therefore, in order develop it, noise measurement data is needed. For this purpose, EPFL is developing a Noise Measurement System (NMS) IC which main objective is to characterize both low frequency and white noise from room- to cryogenic-temperature.

Wireless Wideband Communication and Sensing at Room Temperature

Wideband D-Band RF Switches

Design and simulation of SPDT switch with available compact models have been conducted, the SPDT switch topology is well established and suitable for high frequency switches. The switch has been designed for D-band operation which is from 110-170 GHz. Key parameters of the RF switch include insertion loss (IL) and isolation (ISO) as well as bandwidth (BW). The on-state resistance and the off-state capacitance are important metrics of the transistor that will determine the switch performance. The SPDT switch is useful for finding the limiting factors in the nanowire transistor technology since the well-established topology is easy to benchmark. Schematic of the SPDT switch is shown in Figure 1.

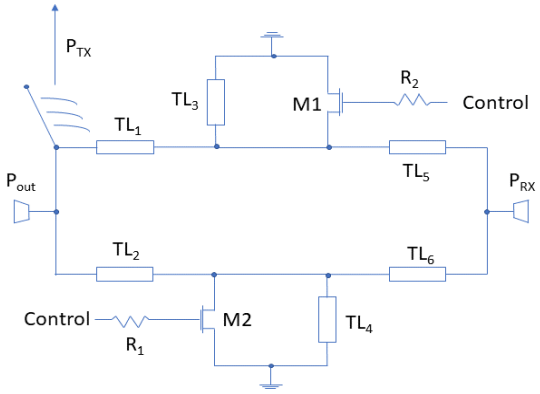


Figure 1: SPDT switch schematic.

In the design a back end of line (BEOL) with 0.5 dB/mm attenuation at 50 GHz is used, this is comparable to what other D-band switches are using. The transistor compact model have a low on state resistance (R_{on}) of 322 Ωμm. The device has a gate length (L_g) of 50 nm.

The D-band SPDT switch simulation results show a bandwidth from 110-170 GHz with Isolation of more than 20 dB for the whole bandwidth and insertion loss is between 1.85-2.65 dB.

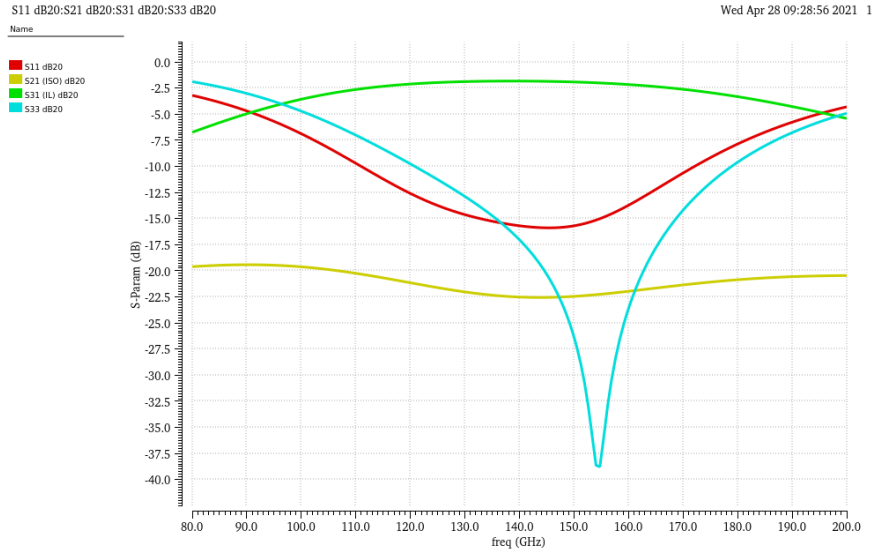


Figure 2: S-parameters of SPDT switch.

Limiting Factors

Performance of the switch is largely determined by R_{on} and C_{off} as well as the transmission line attenuation and Q-value. Focusing on the technology bottlenecks, which with regards to the switch is R_{on} and C_{off}.

The on-state resistance is largely determined by the drain and source resistance of the device. The best reported values of R_{on} for vertical nanowire transistors are 190 Ωμm for a 25 nm L_g DC device [1]. Using 190 Ωμm the switch IL would improve 0.3 dB and the isolation improve around 4 dB.

The off-state capacitance is determined by C_{gd}, C_{gs}, and C_{sd} and will in combination with the inductive stub limit the switch performance with regards to the bandwidth. C_{off} also affect the insertion loss of the switch but the isolation is dominated by R_{on}. Figure 3 and 4 show how isolation and insertion loss change with C_{off} and R_{on}, respectively.

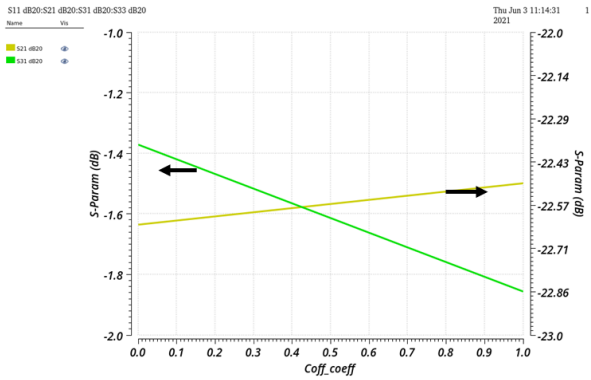


Figure 3: IL + ISO vs Coff.

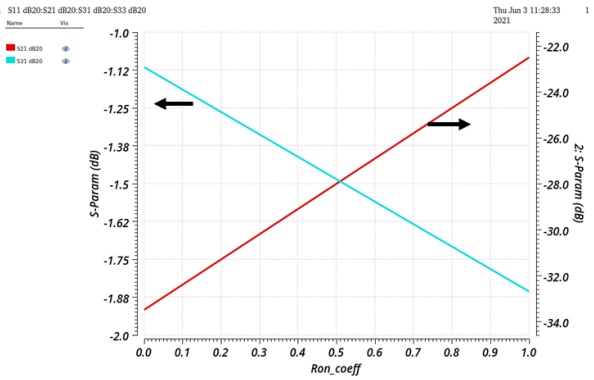


Figure 4: IL + ISO vs Ron.

Low R_{on} and C_{off} is somewhat conflicting requirements in a vertical transistor since, by making the transistor smaller in the vertical direction will decrease Ron since the access regions are shorter, however at the same time C_{off} will increase since the metal contacts are closer together. Scaling of the structure will thus not improve the figure of merit $R_{on}C_{off}$. Instead, other approaches are needed to improve the switch performance in the vertical nanowire technology, such as higher doping in the access regions or lower permittivity dielectrics.

ULUND is working on D-band RF switch circuits under ST4.1.2 of the project. The D-band switch is designed in vertical MOSFET technology and is intended for wideband backhaul in wireless communications. The basic topology of a single pole double throw (SPDT) RF switch based on shunt devices is illustrated by the circuit schematic in Figure 5, inspired by switch design in HEMT technology [2]. Each output branch of the device is initiated by a quarter-wave transmission line section and terminated by a shunt MOSFET. The signal is allowed to pass by biasing the MOSFET in cutoff, providing only a parasitic capacitance on the output that can be resonated out by an inductor. If the MOSFET is biased in the linear region, the conducting channel will short circuit the output and reflect the signal. This reflection is perceived, through the quarter-wave line transform, as an open circuit on the input side.

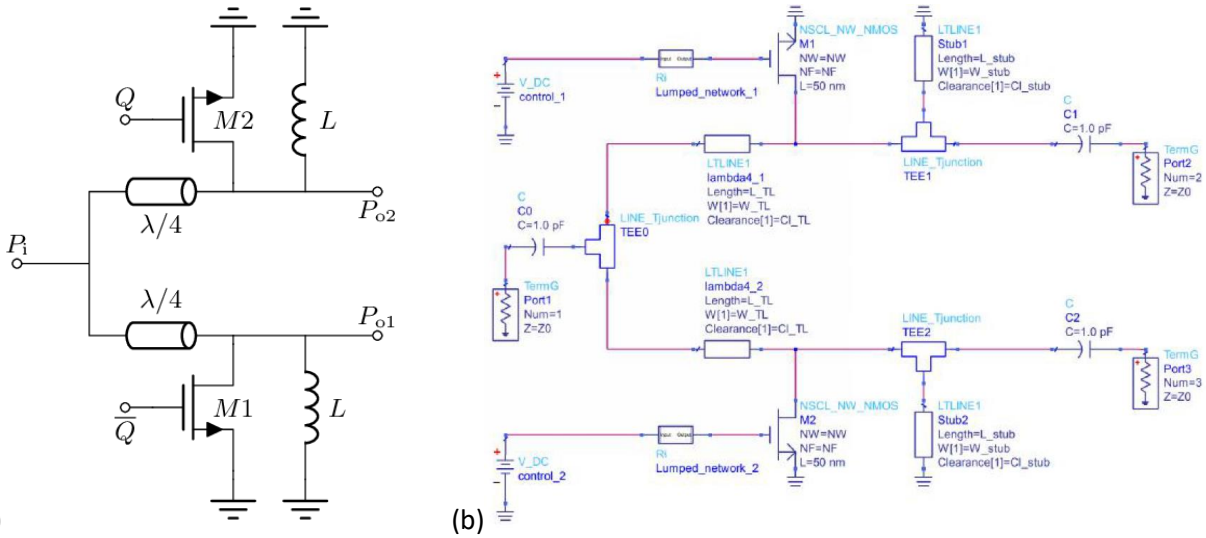


Figure 5: (a) Simplified schematic of the SPDT RF switch based on shunt devices. The inductor on each output branch is tuned to resonate the off-capacitance of the MOSFET. (b) Simulated schematic based on a parametrized design in Keysight ADS.

A design in the D-band is targeted and we have made preliminary simulations of the circuit performance around 120 GHz, as shown in Figure 6. The SPDT switch is seen to cover approximately 40 GHz bandwidth with insertion loss, S21,ON, of only about 3 dB, while providing more than 20 dB isolation, S21,OFF. This design utilizes a vertical MOSFET with 1200 nanowires per device in 5 fingers. We also performed a parameter study for the number of nanowires per device. This illustrates the impact of non-zero conductance and parasitic capacitance in the MOSFET off-state / (branch on). The requirement of a proper short-circuit from the on-resistance of the device forces a large MOSFET. The resulting off-conductance loads the on-branch and generates insertion loss whereas the off-capacitance limits the achievable bandwidth. However, there is also an insertion loss contribution from the off-branch that improves for a larger device.

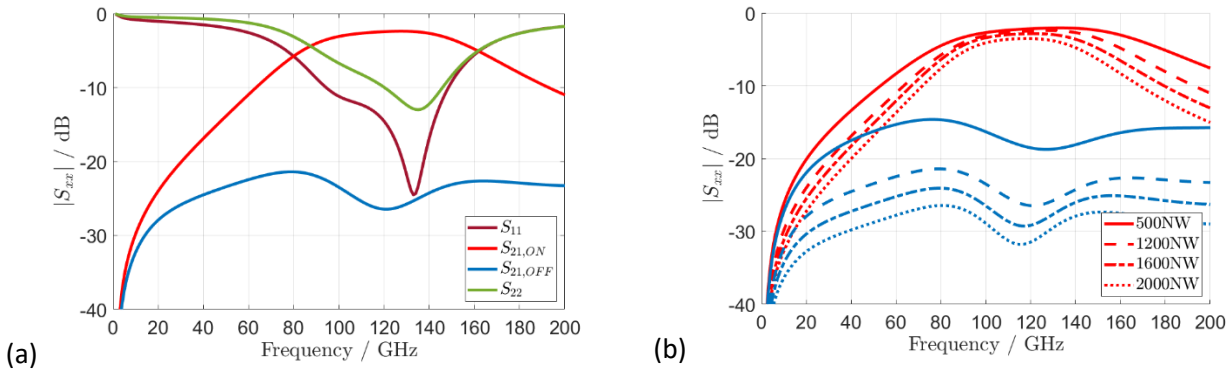
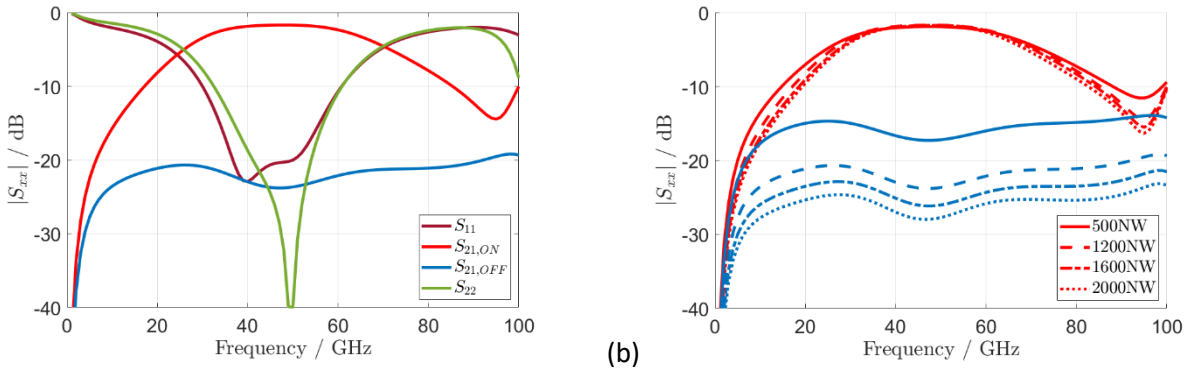


Figure 6: Simulated scattering parameters of the D-band RF switch. S11/22 is the input/ output matching, S21,ON is the gain in the branch, and S21,OFF is the isolation in the branch.

The first design of the SPDT RF switch, although D-band is targeted, is made at 50 GHz center frequency. This makes a good test vehicle for the design process and allows more simple characterization. The simulated performance of the 50 GHz SPDT switch is presented in Figure 7. The results are similar to the D-band design and the average performance metrics are presented in Table 1.



(a) (b)

Figure 7: Simulated scattering parameters of the 50 GHz RF switch. S11/22 is the input/ output matching, S21,ON is the gain in the branch, and S21,OFF is the isolation in the branch.

Table 1: Simulated SPDT switch design results for different device sizes in III-V nanowire MOSFET technology, illustrating the tradeoff between device size, bandwidth, isolation, and insertion loss.

Transistor (NW/NF)	**Topology**	**Fc (GHz)**	**BW (GHz)**	**BWr (%)**	**ISO (dB)**	**IL (dB)**	**FoM (GHz)**
500/5	SPDT	48	25-72	97	16.0	2.8	270
1200/5	SPDT	49	27-71	90	22.3	2.6	377
1600/5	SPDT	49	28-70	86	24.6	2.6	390
2000/5	SPDT	48	32-64	83	26.7	2.3	463

The design kit describes a vertical InGaAs nanowire MOSFET technology with co-integrated back-end-of-line (BEOL) components, illustrated in cross section in Figure 8. It utilizes coplanar transmission lines and with 3D integrated passive devices. One special property of this technology is that the ground bridges typically needed in coplanar technology are instead implemented as underpass connections routed on the substrate. This co-integrated BEOL is a first step towards implementing a shielded front-side BEOL technology, which can provide sufficient performance in sub-THz applications.

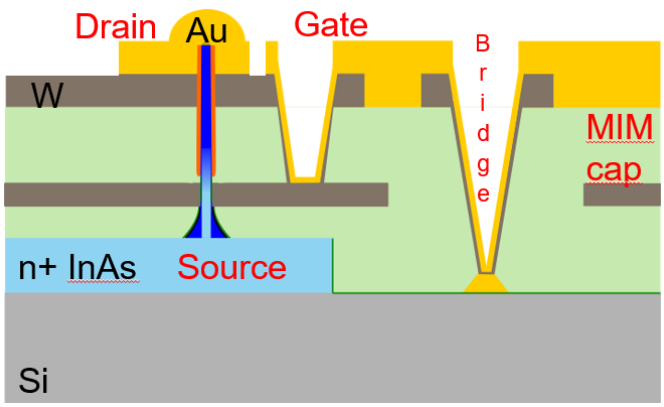


Figure 8: Technology cross section for the vertical nanowire MOSFET process, showing the co-integrated BEOL.

The layout of the 50 GHz SPDT switch is shown in Figure 9, measuring 1.2 mm x 0.9 mm. The input port is located on the left hand side and the two outputs are located on the right hand side. Note that the top right output branch is terminated on-chip to allow a standard two-port measurement.

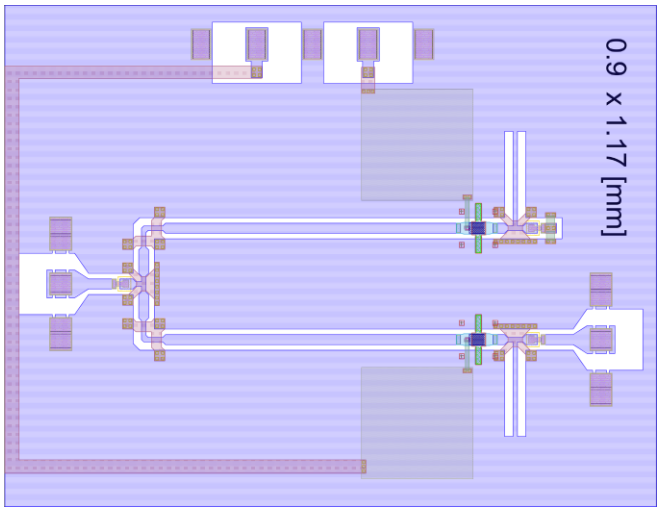


Figure 9: Layout view of the designed 50 GHz RF switch.

Integration of LNAs and RF Switches

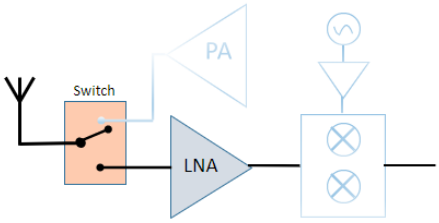


Figure 10: Principal functional blocks illustrating the front-end part of a wideband communication transceiver.

Low Noise amplifier, LNA and antenna switch constitutes the basic building blocks of a wideband wireless communication transceiver. Integrating Switch, LNA and even the PA would offer several signal quality advantages.

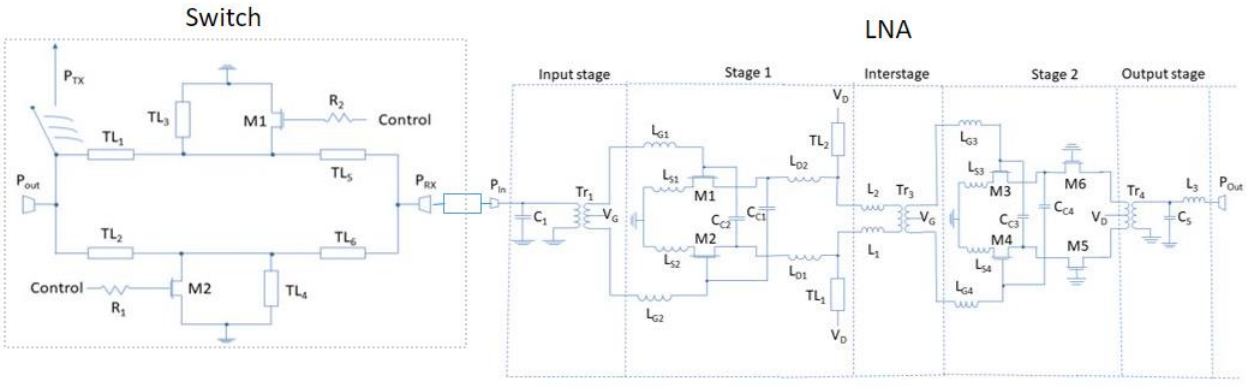


Figure 11: Combined schematic of SPDT switch and a 2-stage LNA design is shown above.

Figure 11 shows the schematic of the combined LNA and SPDT switch designed for 5G applications operating at the D-band optimized at 110 GHz. The first stage is a common source stage, and the second stage is a cascoded stage. The second stage also have resistive feedback from the drain of the common gate to the gate of the common source transistors in order to increase bandwidth.

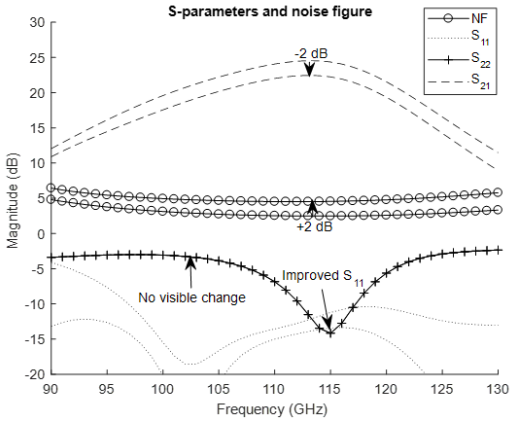


Figure 12: Result comparison for a combined circuit topology of SPDT switch and a 2-stage LNA design and the stand alone LNA circuit is shown above.

Figure 12 shows the change in performance for the S-parameters and the noise figure when a switch is connected to the LNA with 5G applications at 110 GHz. The gain has dropped 2 dB for the LNA connected with the switch in comparison to the single LNA, approximately equal to the insertion loss of the switch. Simultaneously, the switch has increased the noise figure by approximately 2 dB to between 4.8-4.9 dB for the frequency range 106.6-116.6 GHz. The input matching has improved for the LNA that is connected to a switch compared to the single LNA, but there is no change for the output matching.

Summarizing, initial circuit simulation for performance evaluation of integrated LNA + SPDT, yields,

NF = 4.8 dB (2.8 dB)

Gain = 22.5 dB (24.5 dB),

Numbers in parentheses refer to the stand alone LNA results.

Multi-Frequency Signal Generation

The multi-Frequency generation building block is targeting sub-20 GHz communication and then the SPIN Qubit manipulation applications implemented in FDSOI process. The mmW to THz D-Band could also be explored with existing circuit. Even if the multi-Frequency generator will serve the multi-channels communication for 5G, Beyond-5G mobile telecommunication generations. The main difficulty is to serve also the Qubit manipulation. We have, then, decided to focus the specifications of this building block demonstrator to this application.

Specifications:

The first remark is that such circuit will not be implemented at the cryogenic temperature, the power consumption and complexity of the system requiring to be at ambient temperature for heating dissipation, and proximity with the human.

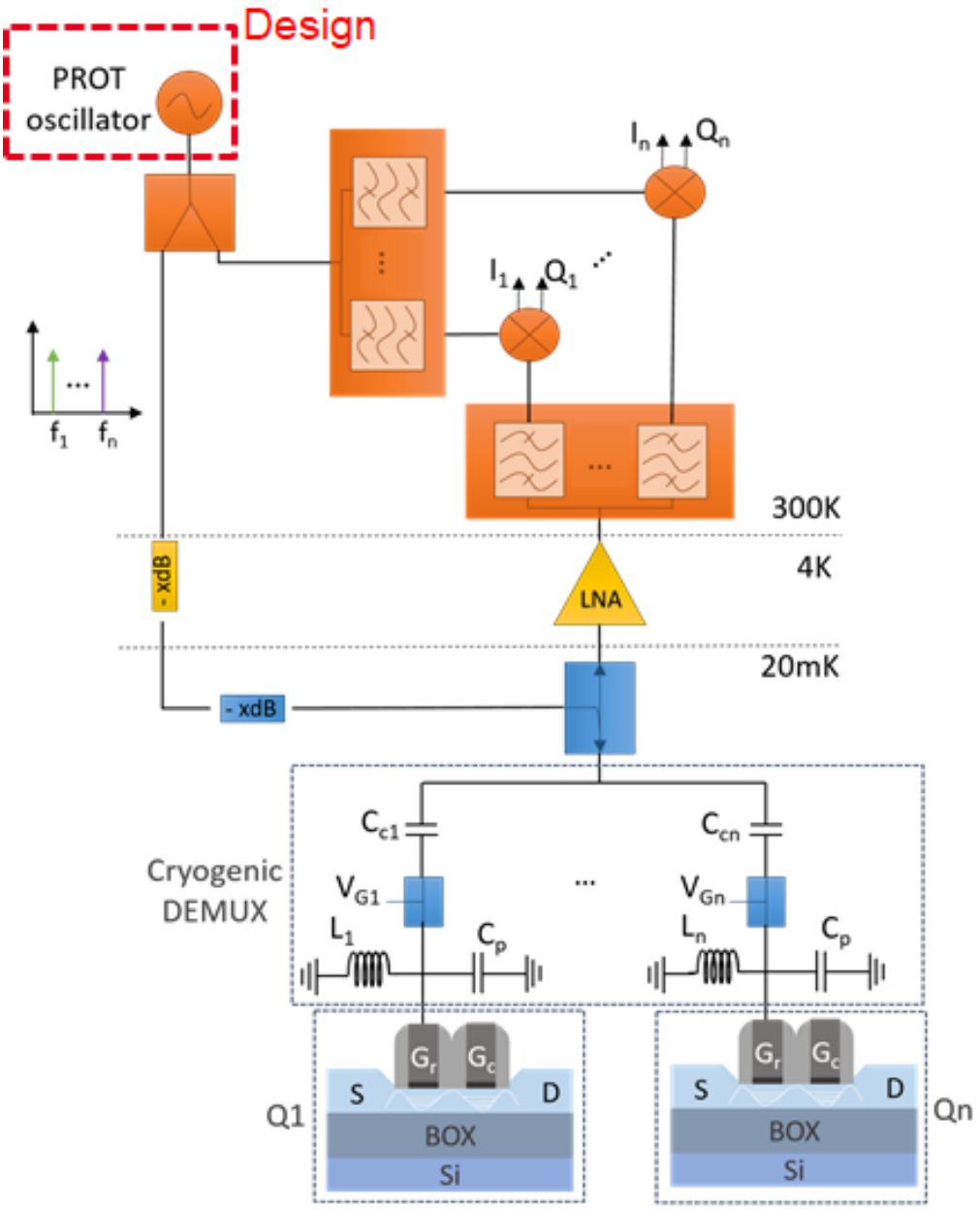


Figure 13: Qubit readout synoptic with the multi-frequency generator (red square).

This system is a scalable approach for multi-qubits readout using a cryogenic frequency multiplexing to reduce the number of cables going down in low temperature stages. That implies the need of a multi-tone frequency generator.

The Multi-frequency generator delivers a signal composed by n harmonics at n frequencies (f1 … fn), with constant steps between each other. The signal is splitted into 2 parts, one is going down to 20 mK cryogenic temperature and control the n qubits, each one is controlled by one harmonic. Thus, the parasitic capacitor of the single electron transistor slightly varies depending on the SPIN position of the electron, this affects the frequency feedback. All the qubits' feedback signals are going up to the ambient temperature through a wide band LNA (at 4 K). These signals are parallelly filtered, in order to orient f1+df1 to fn+dfn to the good paths, at ambient temperature. At the output of the multi-frequency generator, the second path at the output of the splitter is parallelly filtered to orient f1 to fn to the correct path. Then a comparison between f1 and f1+df1 to fn and fn+dfn gives df1 to dfn values representing the n qubits states, when measuring. The operation can

be done continuously, and pseudo-random addressee can be done to improve statistic robustness of the measure.

For this prototype, we focus a 6 frequencies signal from 2 to 4.5 GHz with 500 MHz spacing. This could be in second time extended to a bigger number of frequencies, up to 20 GHz. But the concept demonstration will be easier to validate in such approach, and can be also directly used for 6 qubits quantum computer, under development in LETI. We have to minimize the ΔdBV between frequencies to have a relatively flat frequency profile.

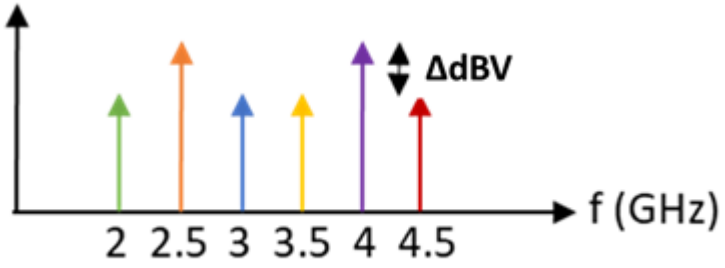


Figure 14: Frequency profile to reach.

The circuit will be designed in GF 45 RF-SOI process, which presents the best compromise to have high quality factor passives components, due to high resistive substrate, and low parasitic transistors with high gm in the frequency range.

Prototype Oscillator Principle:

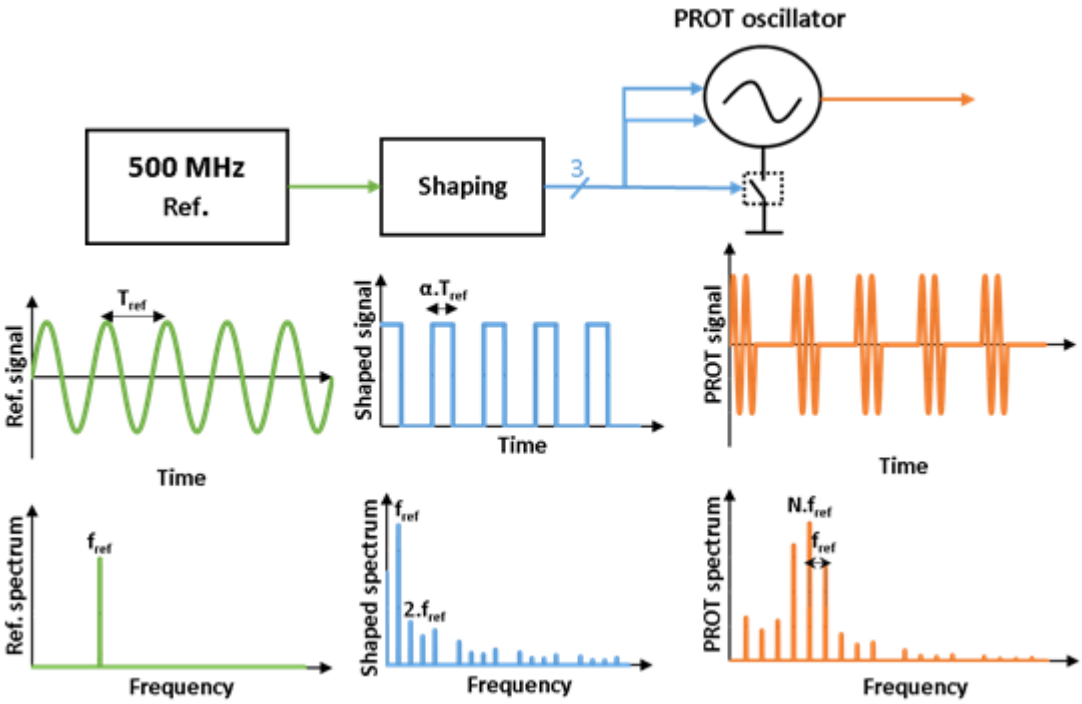


Figure 15: Oscillator Principle.

A 500 MHz reference signal is shaped into a square signal with adjustable duty cycle α. The shaped signal REF periodically turns-on/off the Prototype oscillator in order to generate a frequency harmonics spectrum. This spectrum is centered on the Prototype oscillator free-oscillation frequency (nth harmonic of the reference

signal). The harmonics spacing corresponds to the reference signal frequency. The width of the spectrum and consequently the flatness of the frequency profile is determined by the duty cycle α.

Prototype Oscillator Design:

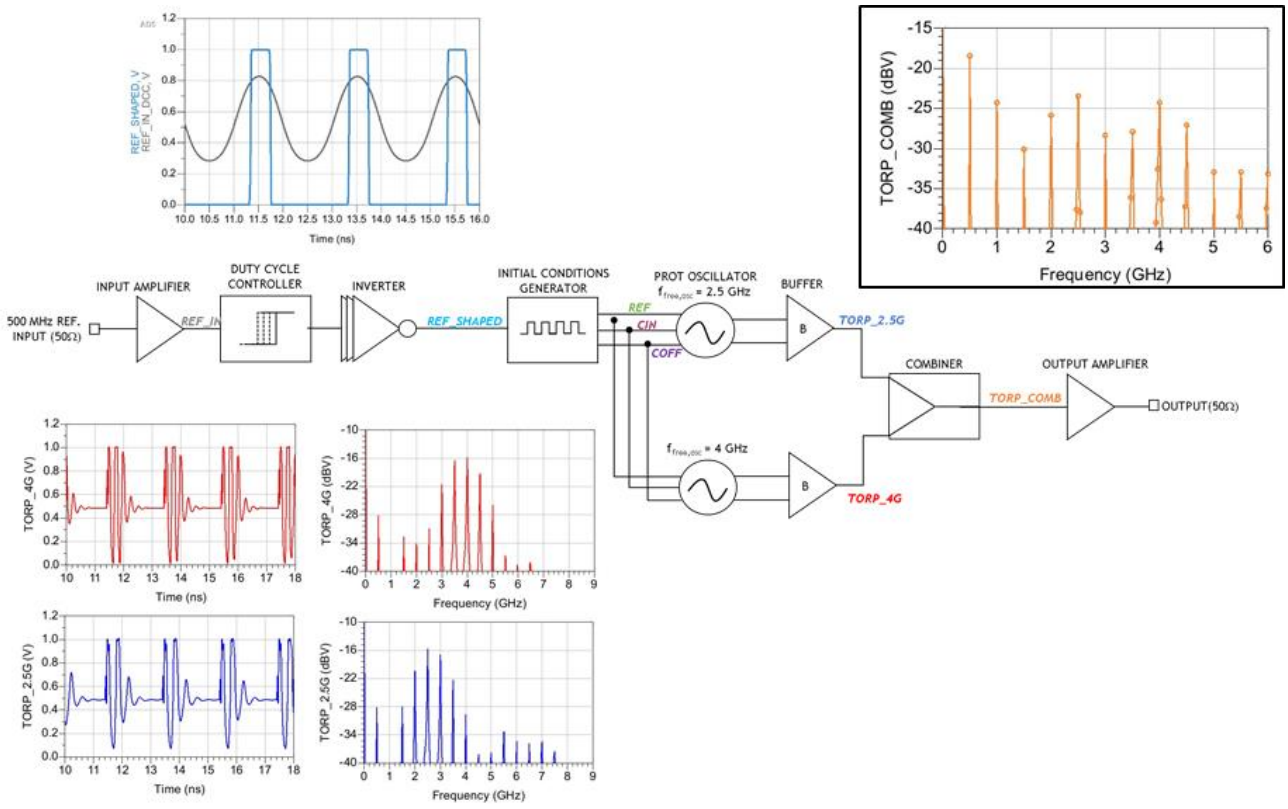


Figure 16: Oscillator schematic and simulations.

As it was exhibited in Figure 15, the main issue of the oscillator principle is the big variation of the amplitudes of the harmonics. This would be solved, to be compliant with what is requested by the frequency profile to reach to serve the qubits readout system presented in the Figure 13.

To minimize the dBV difference between harmonics, we need to combine at least two different frequency signals coming from two different oscillators, the summation of both harmonics from each of them, in a cleaver choice, can compensate the natural variation of one oscillator output. This is what is done in our prototype.

The final set of simulations presented in Figure 16 give the best compromise for small amplitude variation in the 2 - 4.5 GHz range, with a Low duty cycle (α=0.2) and a combination of two oscillators operating at 2.5 GHz and 4 GHz.

The final schematic is given in this Figure 16.

Layout:

Technology: GF 45SOI (run june 2021)

The Layout is ongoing (end of May), and the circuit will be sent to fab end of June 2021. This implies measurements in Q4 2021 or early 2022.

Wireless Space Communication and Sensing at 40 – 70 K

Quadrature LO signals for the RX and TX chains

Satellite communication at E-band, i.e., at 71-76 GHz and 81-86 GHz offers 10 GHz of RF bandwidth [3], thereby enabling a channel with very high capacity. The frequency bands for space-to-earth and earth to space are listed in Table 2 [4]. Fixed point-to-point communication at E-band frequencies is today already used in the mobile backhaul for base stations. Due to the higher carrier frequency, an E-band antenna provides more antenna gain for a given physical size. However, the quality of the E-band link is negatively affected by bad weather conditions, such as rain or fog. The drawbacks can be mitigated by techniques as hub site diversity, adaptive coding and modulation and automatic output power control [3]. To maintain a sufficient quality of the channel, a high Effective Isotropic Radiated Power (EIRP) is required. This can be achieved by utilizing antennas with high directivity or power amplifiers with large output power.

Table 2: Frequency bands for E-band satellite communication.

Space to Earth 71-76 GHz & Earth to Space 81-86 GHz

Allocation to services		
Region 1	**Region 2**	**Region 3**
71-74	FIXED FIXED-SATELLITE (space-to-Earth) MOBILE MOBILE-SATELLITE (space-to-Earth)	
74-76	FIXED FIXED-SATELLITE (space-to-Earth) MOBILE BROADCASTING BROADCASTING-SATELLITE Space research (space-to-Earth) 5.561	
81-84	FIXED 5.338A FIXED-SATELLITE (Earth-to-space) MOBILE MOBILE-SATELLITE (Earth-to-space) RADIO ASTRONOMY Space research (space-to-Earth) 5.149 5.561A	
84-86	FIXED 5.338A FIXED-SATELLITE (Earth-to-space) 5.561B MOBILE RADIO ASTRONOMY 5.149	

Historically, QPSK modulation has been used for satellite communication due to the low SNR requirements. However, to make the best use of the available E-band spectrum, i.e., to increase the spectral efficiency, it is desired to move to higher modulation orders such as 64 QAM or 256 QAM. The high the modulation order, the harder are the requirements on the phase noise of the LO-signal though.

Several architectures for LO generation have been evaluated. The preferred architecture depends on

- Operating frequency
- Key performance of devices in the semiconductor process
- Radio system requirements, e.g., EVM and spurious emission
- Cost, e.g., power consumption, die area and integration level

The direct conversion topology [5], [6], depicted in Figure 17, is an attractive architecture for carrier generation at low frequencies. However, at 84 GHz, it is difficult to design a QVCO, since the Q-value of the varactor is proportional to 1/f, resulting in a high phase noise. The I/Q imbalance due to mismatch in capacitive parasitics will be severe.

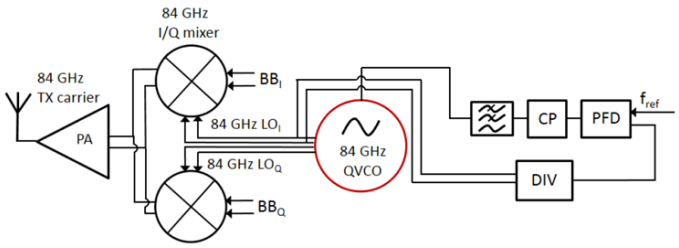


Figure 17: Direct conversion LO signal generation.

Another way to generate the 84 GHz LO signal would be to use a 28 GHz QVCO followed by tripler circuits [7] as shown in Figure 18.

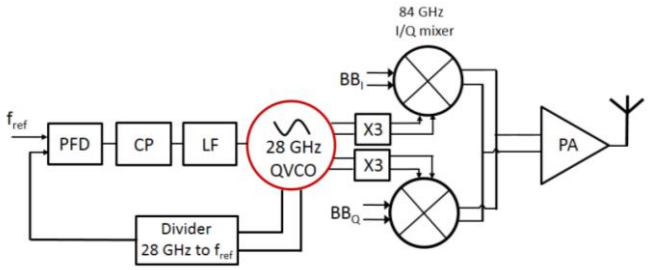


Figure 18: LO signal generation using frequency triplers.

Operating the QVCO at a lower frequency gives lower phase noise and a lower input frequency to the frequency divider thereby reducing the design complexity of this block. The tripler circuits can be implemented as injection locked frequency triplers (ILFT) or harmonic based (HB) triplers. However, both topologies have a high power consumption and generate lots of spurs.

The selected architecture is illustrated in Figure 19. Only the TX chain, [8], [9] has been simulated. It is based on a 28 GHz QVCO generating I/Q signals for a first upconversion of the baseband signals. The second order tail harmonic present at the source terminal of the QVCO core devices is used as LO signal for the second mixer. Operating the QVCO at lower frequency gives improved I/Q balance, phase noise and tuning range. No frequency tripler circuits are required.

The RX chain is similar, but with mixer order reversed, i.e., the RF signal is first down converted to 28 GHz in a single mixer supplied with a 56 GHz LO signal. Down conversion to baseband signals is thereafter performed in an I/Q mixer driven by quadrature 28 GHz LO signals. Since the TX chain is fully functional, we decided to postpone the work with the RX chain.

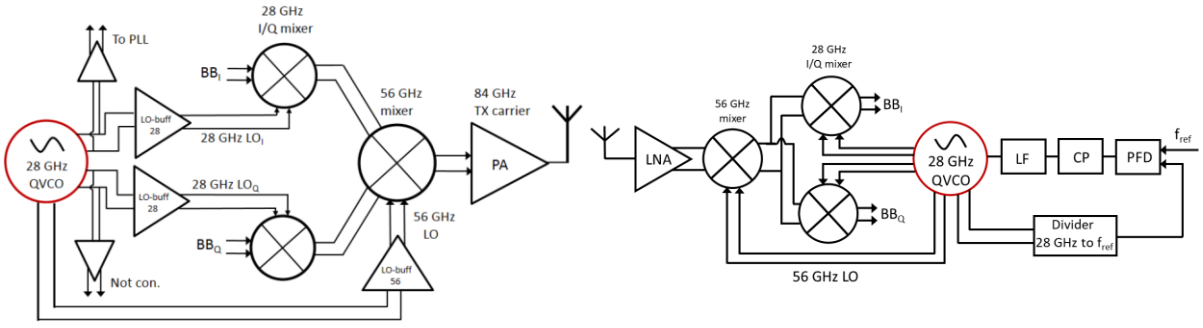


Figure 19: (a) TX LO signal generation (b) RX LO generation.

No simulations below room temperature have been performed due to lack of device models with temperature dependence. We have focused on the room temperature performance of the LO topology. Main design goals have been to establish a schematic were the device sizes, signal levels and bias currents have been optimized to deliver an acceptable performance. An important part of the design are the 28 GHz and 56 GHz LO driver buffers for the mixers since these blocks define the wave form and of the driver signals.

The TX LO chain signals levels assumes a power amplifier (PA) with at least 20 dB gain. Base on previous studies, this is a reasonable assumption. Using a 1.5 V supply, the current consumption is the following:

- 28 GHz I/Q mixer (both): 16 mA (8 + 8 mA)
- 56 mixer: 23 mA
- 28 GHz LO buffer (both): 11 mA (5.5 + 5.5 mA)
- 56 GHz LO buffer: 3.2 mA
- Total: 53 mA of mixers + buffers

The 28 GHz QVCO defines the phase noise and tuning range of the architecture. The phase noise is determined by the noise from resonance tank, i.e., the varactor and inductor, plus the noise of the active devices. In the simulations, the inductor has a Q-value of 18 at 28 GHz, reflecting the properties of the metal stack, while the varactor has a Q-value of around 50 depending on tuning voltage. To maximize the tuning range, it is beneficial if the fixed capacitances of the active devices and the varactor are small. However, the tuning range of the carrier is three times larger than the tuning range of the QVCO, thereby relaxing the requirements. The actual requirement of the QVCO tuning range also includes process spread. The QVO including two resonance tanks, the two coupled active VCO cores, the 56 GHz output transformer and the DC biasing devices are shown in Figure 20 below.

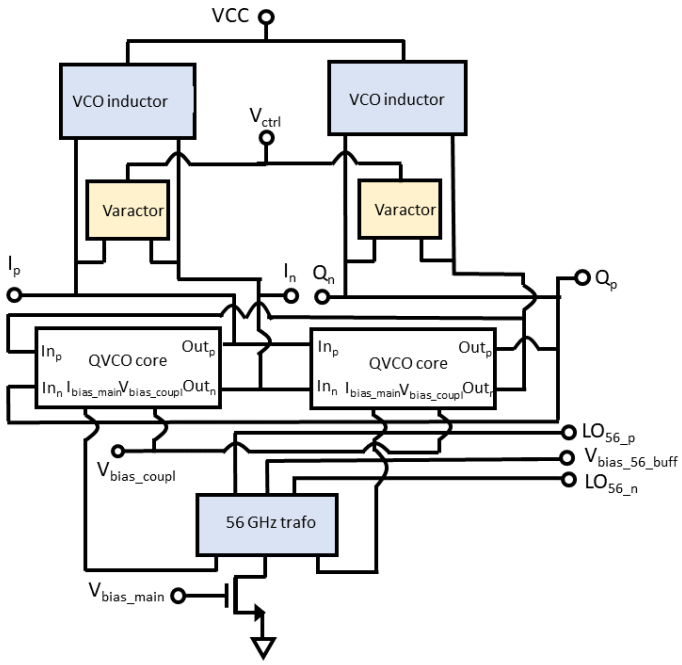


Figure 20: QVCO architecture.

The QVCO core consisting of main and injection devices is depicted in Figure 21. The main devices (to the right) and the injection devices (to the left) are sized with 100 wires and three fingers. The phase noise

depends on the bias current ratio between the injection and the main devices. In Figure 21, the main tail current equals 9.8 mA, while the injection tail current equals 3.4 mA.

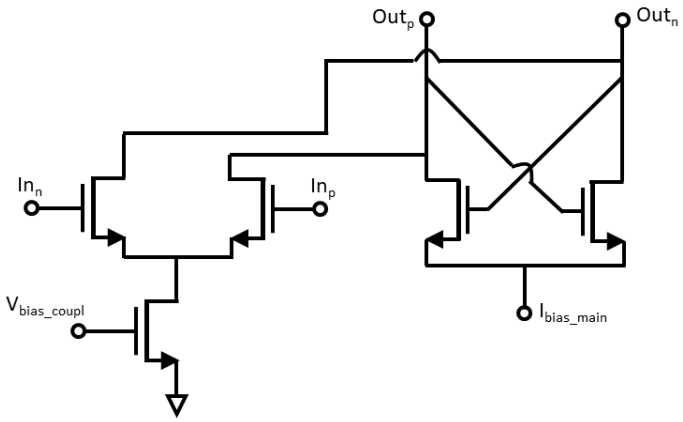


Figure 21: QVCO core.

The varactor devices, depicted in Figure 22, consist of 3900 wires grouped into 50 fingers to increase the Q-value. With this scaling, Q is equal to 45 at the tuning midpoint.

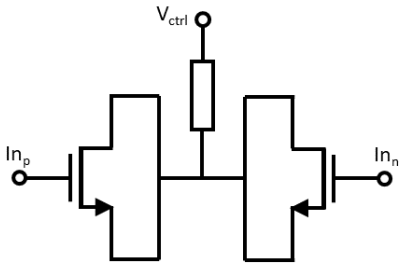


Figure 22: Varactor.

The waveforms of the two differential QVCO 28 GHz outputs plus the differential 56 GHz output are shown in Figure 23.

- Differential 28 GHz output voltage swing = 1.4 V
- Differential 56 GHz output voltage swing = 0.66 V

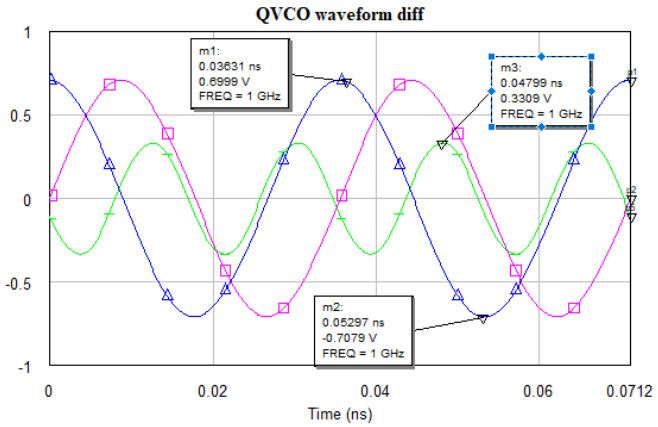


Figure 23: QVCO waveforms.

The phase noise versus frequency curve is given in Figure 24. At 1 MHz offset from 28 GHz, the phase noise equals -86 dBc/Hz.

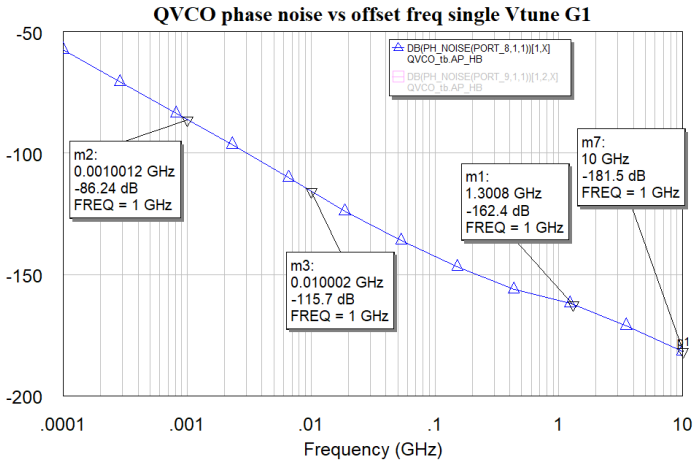


Figure 24: QVCO phase noise.

Mixer Design

The full mixer architecture consists of three mixer cores with individual LO buffers as previously shown in Figure 19. Assuming a 20 dB gain of the PA the output power of the mixer will need to be in the range of -5 dBm while achieving a reasonable linearity. Double balanced mixer topology has been chosen for the mixer design of the transceiver. The mixer core is shown in Figure 25. A double balanced topology will reduce the LO and IF leakage for the upconverting mixer (LO and RF leakage for the down converting mixer) [10]. The differential output will reduce the even order intermodulation products. An important feature of the double balanced mixer is that noise from the LO driver is suppressed.

In order to have the switching transistors of the mixers operating correctly and to achieve sufficient isolation to the QVCO, LO buffers are necessary and should not be overlooked in the design process.

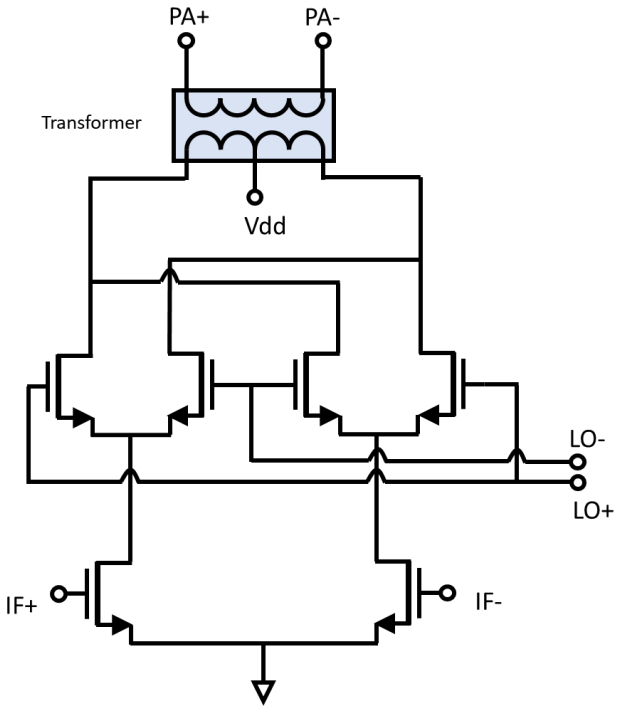


Figure 25: Schematic of the mixer core.

A saturated output power of 1.17 dBm and 1-dB compression point of -3.5 dBm is shown in Figure 26. Assuming a PA stage with around 20 dB this output power from the mixer should be sufficient.

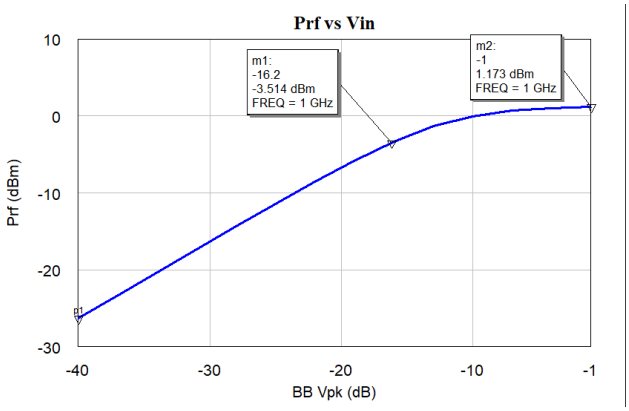


Figure 26: RF output power vs baseband input voltage.

The bandwidth of the mixer is shown in Figure 27 and is 80.7-88.7 GHz, which covers the E-band, however additional bandwidth is needed in the mixer in order not to put harder requirements on the performance of the PA. A larger margin of bandwidth is also important to account for process spread.

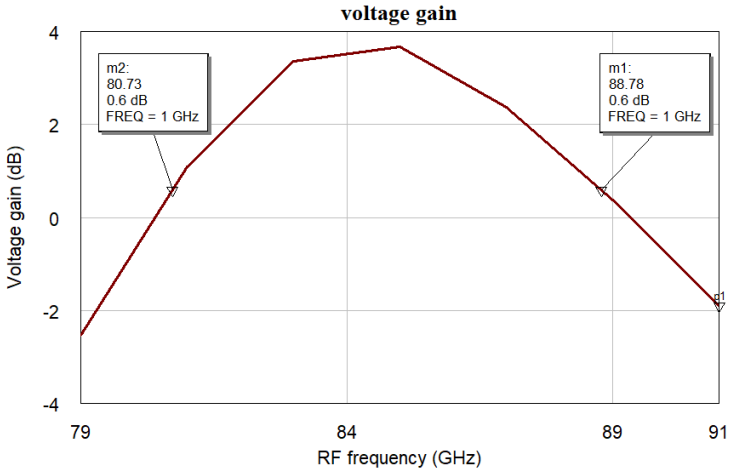


Figure 27: Voltage gain vs RF frequency.

Two tone simulations of the mixer with baseband frequencies of f1 = 1 GHz and f2=1.1 GHz have been conducted and the results are shown in Figure 28. Output third order intercept point is found to be 6.7 dBm. OIP3 is then 10 dB higher than the 1-dB compression point of the mixer.

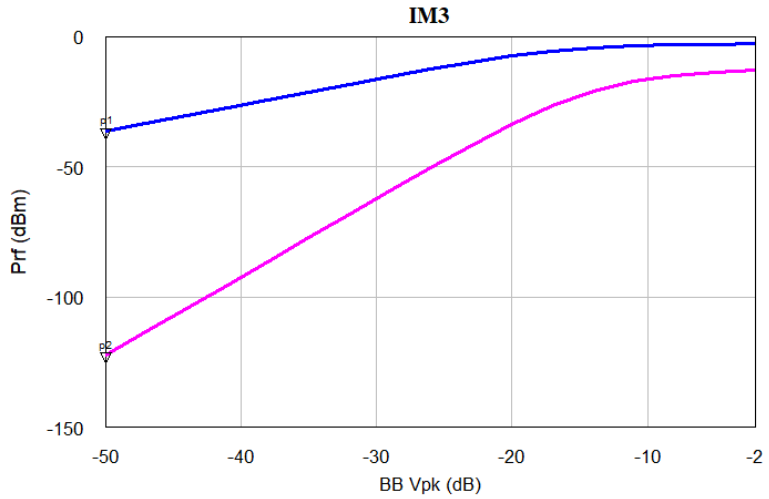


Figure 28: Third order intermodulation product vs baseband input voltage.

Initial design of the mixer is completed, there are minor issues with regards to bandwidth. Further optimization of the circuit is possible. Mixer linearity is a key parameter and needs to be investigated further.

Similar mixer topology with small changes can be used for the receiver and for the 71-76 GHz band.

The transistor model used for the initial design is validated for room temperature simulations, further modelling work is required in order to accurately model lower temperatures. Temperature dependence will be looked in to at the later stages of the project.

E-Band RF Switches

ULUND is working on E-band RF switch circuits under ST4.2.2 of the project. The E-band switch is designed in III-V vertical nanowire MOSFET technology on Si and is intended for satellite communications [11]. These switch circuits will be based on the same design concepts as those developed for D-band operation. However, the lower operation frequency may allow more sophisticated design variations. For example, the regulations in the E-band that stipulate two bands (downlink 71-76 GHz and uplink 81-86 GHz) separated by a guard band. This provides additional design opportunities for the antenna switch. The switch branches can be adapted to the different bands, which are interchanged at the two sides (earth and space) of the link. Work on the E-band switches is pending progress in the D-band design, as described above, where initial development of the design flow and process verification is performed.

E/W-Band LNAs and RF Switches (IAF)

In Subtask 4.2.3, IAF is working on an integrated solution of a single-pole double-throw (SPDT) switch and an LNA. The major target is an operating frequency of 89 GHz. However, it is the goal to cover as much as possible of the entire W-band (75 – 110 GHz) without compromising the 89 GHz performance considerably. A simplified schematic of the Switch + LNA MMIC is depicted in Figure 29. The switch is based on a quarterwave transmission line transformation topology in a coplanar waveguide transmission line environment. The 50 nm Schottky mHEMTs are connected in shunt configuration (parallel to the transmission line). The RF ports of the switch are RF coupled to the RF input of the MMIC and to the LNA input. The LNA is based on a four-stage common-source topology. Each stage features a four-finger HEMT with a total gate width of 48 µm. All stages use an inductive source degeneration concept. In the first stage, the source degeneration is used for a simultaneously improved input noise and power matching of the LNA. In the later stages, it is used for an improved wideband frequency response. In the stages two to four, small resistors in the drain path ensure unconditional stability. In the first stage, only a small resistor is used in the drain path to avoid a detrimental

impact on the noise performance of the LNA. The shorted stubs in the gate, drain, and source matching networks of the LNA use high-impedance transmission lines (close to the technological limit), which further improves the wideband frequency response. The Design of switch and LNA is optimized for the targeted temperature range of approximately 50 K. The simulation are done with the temperature dependent small-signal model that was described by our group in D2.2.

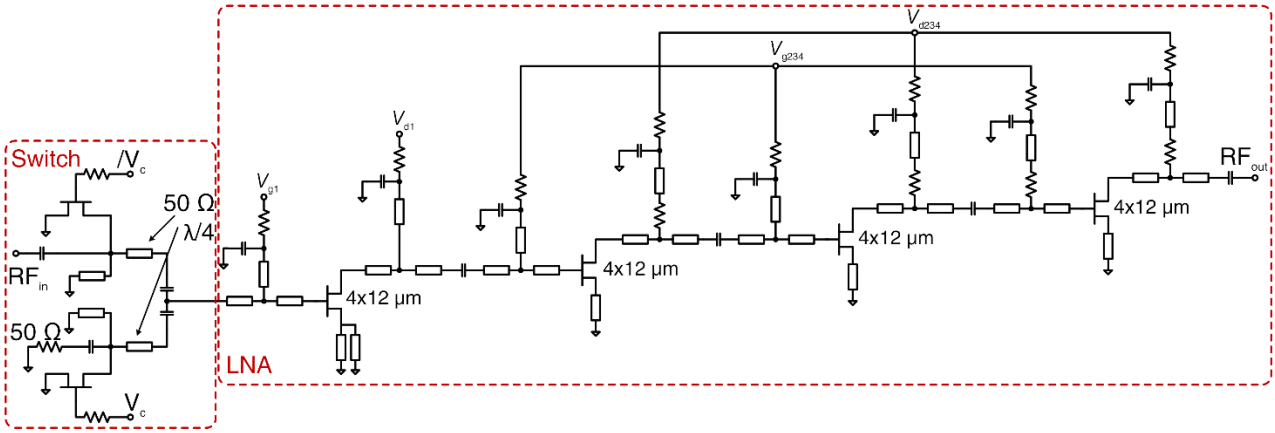


Figure 29: Simplified schematic of the integrated circuit SPDT switch and LNA.

The simulation results of the SPDT switch as a stand-alone circuit are shown in Figure 30 for room temperature and for an ambient temperature of 50 K. The switch is fully EM simulated. The insertion loss is about 1 dB at T = 297 K and improves by approximately 0.2 dB when cooling the switch to 50 K. The isolation is better than 30 dB. The input and output return loss better than 10 dB for the entire W-band and better than 20 dB for the 89-GHz frequency range.

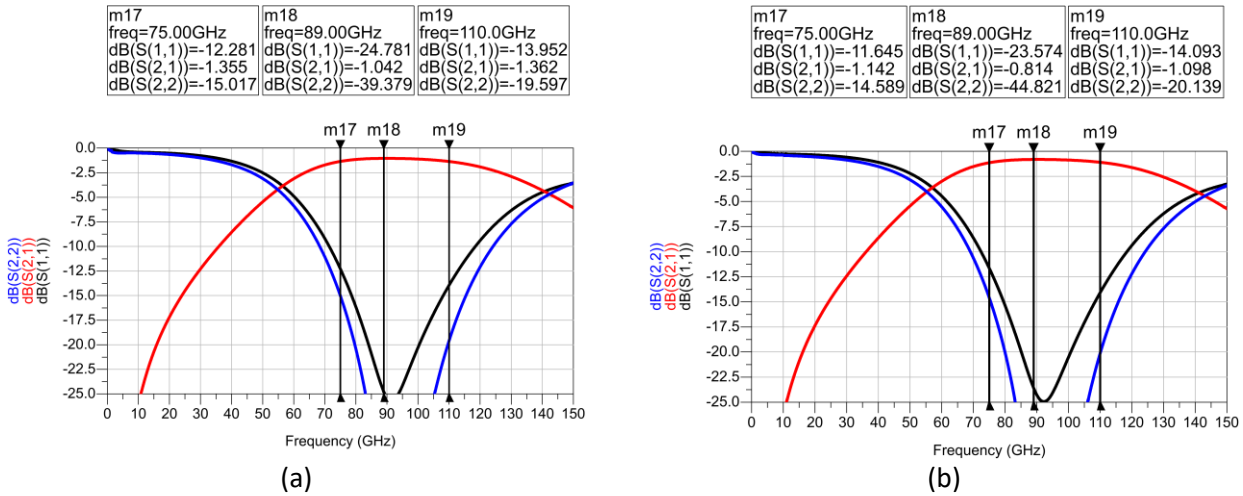


Figure 30: Simulated S-parameters of the switch stand alone at (a) room temperature and (b) 50 K.

The simulated LNA performance at room temperature and at an ambient temperature of 50 K is given in Figure 31. For the major part of the W-band, the input and output return loss are better than 10 and 15 dB, respectively. The small-signal gain is better than 25 dB. At room temperature, the noise temperature is in the range of 130 – 160 K. When cooled to an ambient temperature of 50 K, the noise temperature improves to values in the range of 31 – 38 K.

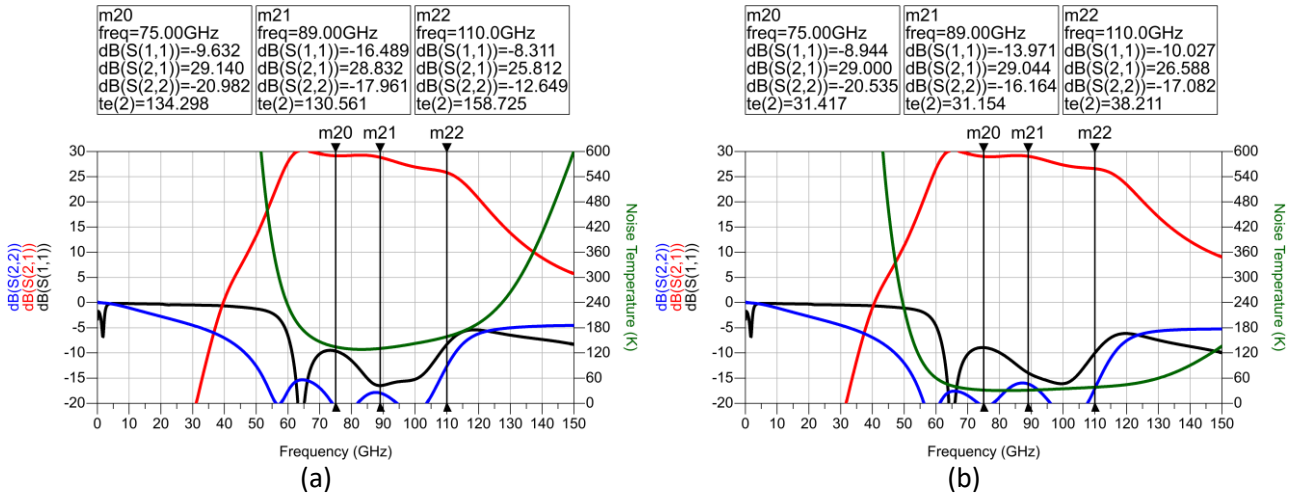


Figure 31: Simulated S-parameters and noise temperature of the LNA stand alone at (a) room temperature and (b) 50 K.

The simulated performance of the combination of SPDT calibration switch and LNA is shown in Figure 32. The small-signal gain is still above 25 dB for the major part of the W-band. The input and output return loss are better than 10 and 15 dB, respectively. At the 50-K temperature range, the noise temperature is about 80 – 90 K.

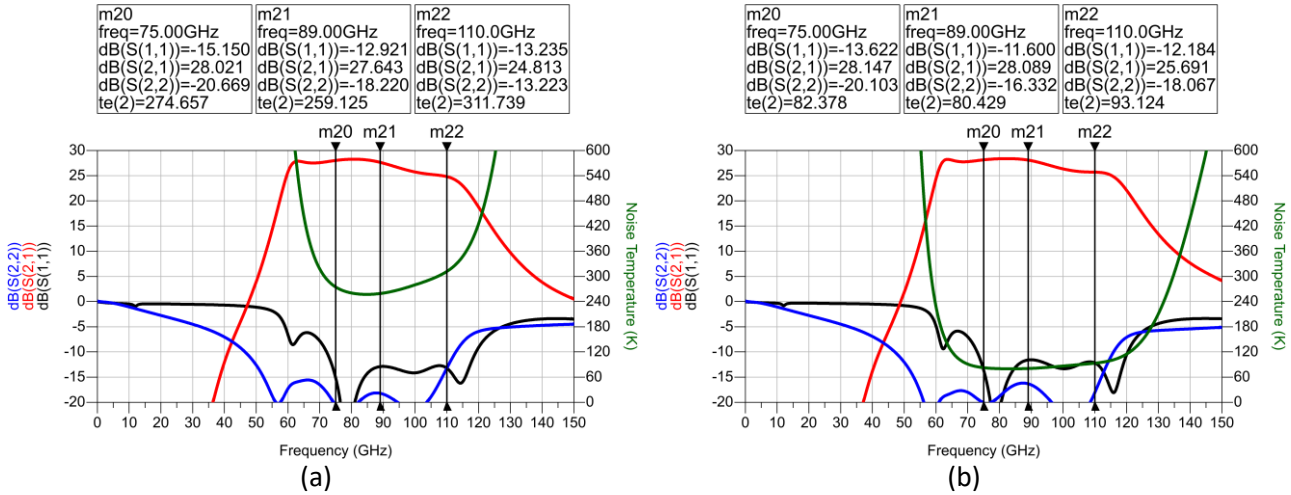


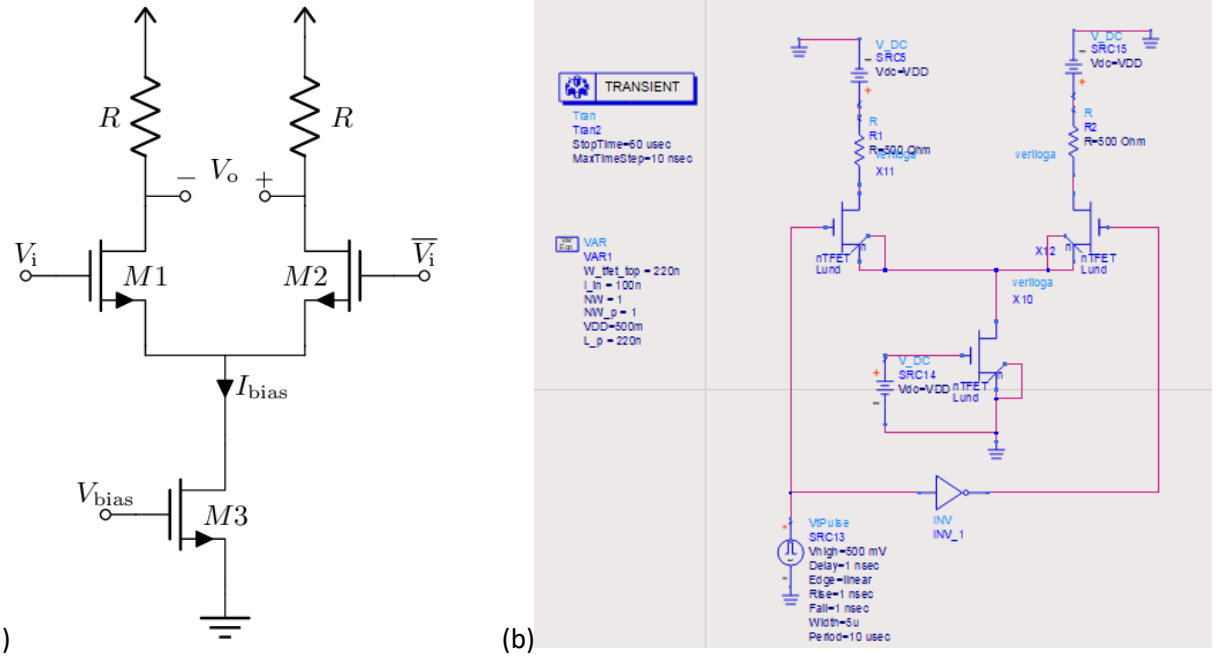
Figure 32: Simulated S-parameters and noise temperature of the monolithic integration of switch and LNA at (a) room temperature and (b) 50 K.

Cryogenics Logic and Mixed Signal Circuits

III-V nanowire FET Digital Circuits (ULUND)

ULUND is working on energy efficient logic circuits under ST4.3.3 of the project. The circuits are designed in III-V nanowire TFET technology on Si and is intended for RF front-end integration. Single or few wires per device are used to implement energy efficient current mode logic (CML). Source coupled CML with n-type TFET devices allow fast, relative to CMOS logic, and efficient, relative to MOSFET devices, operation. Under predictable quiescent periods, where CML would draw unnecessary bias power, the bias can be turned off. One application example is data processing in the receiver channel of a low duty cycle pulsed radar.

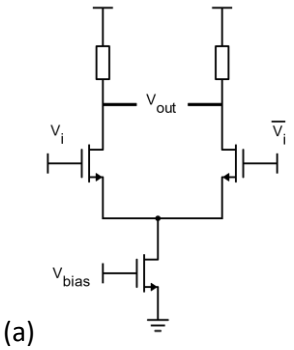
The implementation of a CML inverter is shown in Figure 33. Resistors are used as loads in the two differential branches that share a current sink at the sources of the inverter devices.



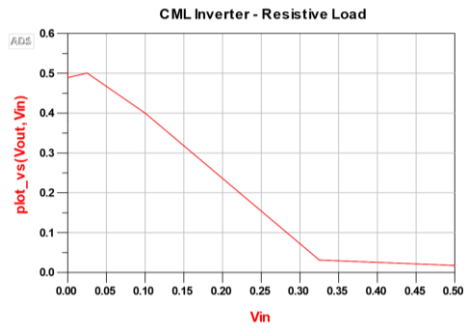
(a) (b)

Figure 33: (a) Simplified schematic of the CML inverter and (b) simulated schematic of the CML inverter.

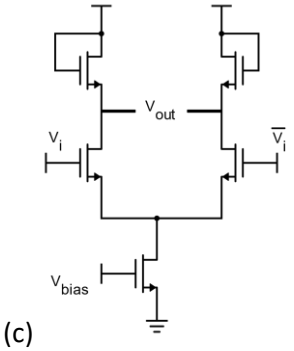
Different types of load implementations in the TFET source coupled CML inverter branches can also be considered. We focus the first design on a 100 kΩ resistive load (for full voltage swing), but also consider the cases of diode connected TFET and PMOS active load. A comparison of the designs and their voltage transfer characteristics for different load types is presented in Figure 34. The diode connected TFET load allows for a simpler, compact, implementation of the CML inverter based on TFETs only. The PMOS active load yields better performance, as compared to the resistive and diode connected TFET load configurations.



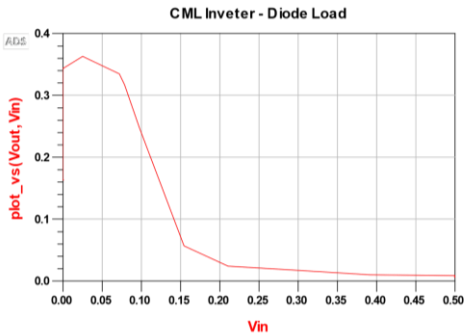
(a)



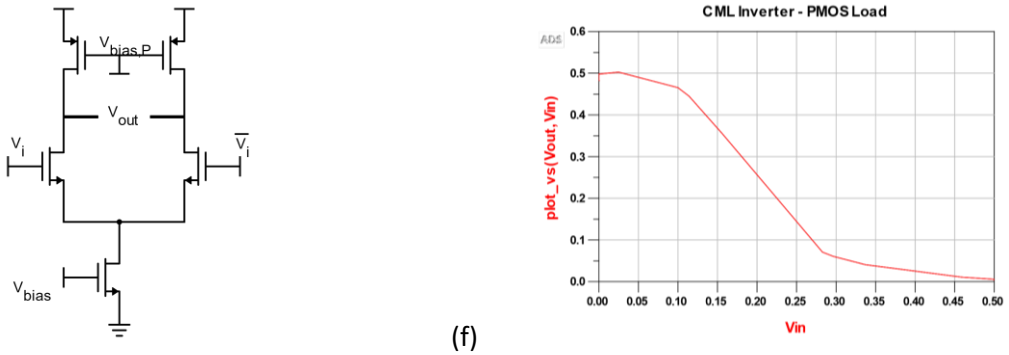
(b)



(c)



(d)



(e) (f)

Figure 34: Simulated voltage transfer characteristics of the TFET source coupled CML inverters, comparing designs using (a-b) resistive, (c-d) diode connected TFET, and (e-f) PMOS active loads.

Dynamic behavior of the CML inverters are shown in Figure 35, where the output can be seen to invert the 100 kHz square wave input. These designs are implemented with full, or as high as possible, voltage swing as a design criterion. Note that this is not a strict requirement for CML logic, where the switching of current between the branches is the core functionality.

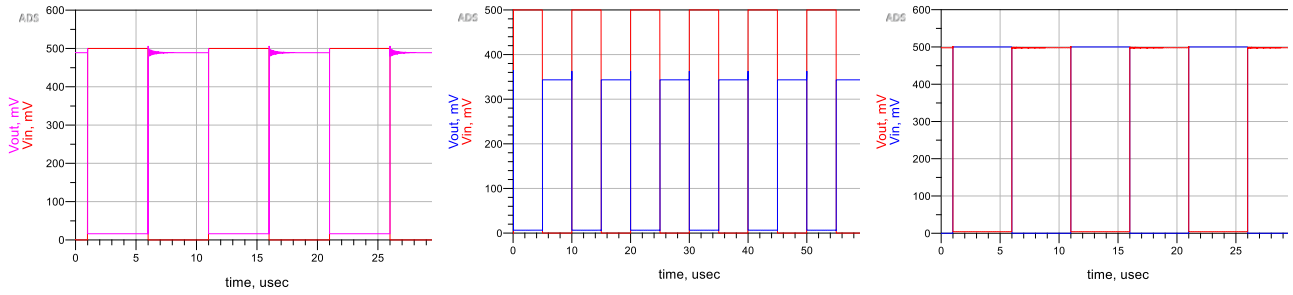
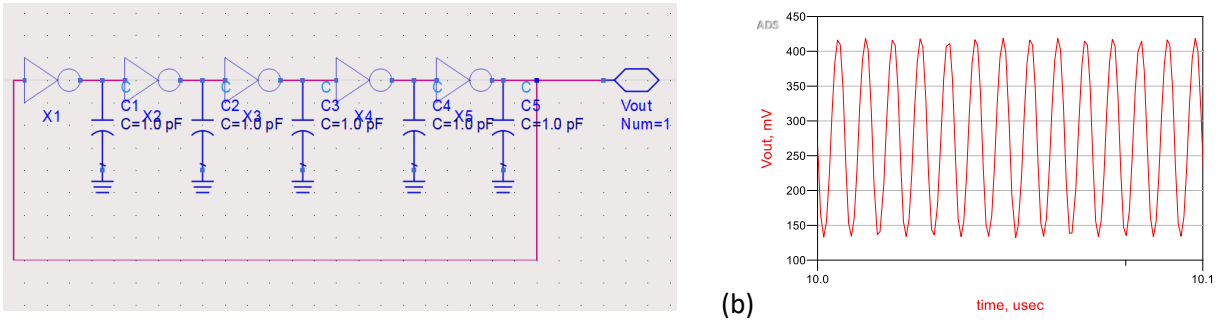


Figure 35: Simulated voltage waveforms of the TFET source coupled CML inverters, comparing designs using (a) resistive, (b) diode connected TFET, and (c) PMOS active loads.

As a standard test for the TFET source coupled CML inverters, presented in Figure 36, a 5-stage ring oscillator is implemented in the simulation environment. Shunt 1-pF capacitors are used to model the interconnects and oscillations are observed for all of the designs. It is also noted that the resistive load inverter can operate at higher speed if the load resistance value is decreased, what will be discussed below.



(a) (b)

Figure 36: Simulated III-V nanowire TFET source coupled CML ring oscillator. (a) Schematic circuit view and (b) example voltage waveform from the inverter design using 1 kΩ resistive load.

A summary of the ring oscillator simulation results is presented in Table 3. The oscillation period the ring oscillator with PMOS active load is simulated to be 120 ns, corresponding to an operation frequency of 8.4 MHz. This corresponds to a 12 ns single stage propagation delay in the 5-stage ring oscillator, which is the fastest result of the designs presented in static simulations above.

Since we are working in current mode configuration, it provides us with an extra flexibility in design. As long as the logic output (0 and 1) can be mapped to the next stage, the voltage levels of the output doesn't matter.

For instance, the output voltage for 1 kΩ and 100 kΩ resistive load CML inverter is shown below. Though the output voltage levels is affected, the logic is maintained. When we exploit this to make ring oscillators, we observe increase in output frequency from 0.9 MHz to 143 MHz. Likewise, we can change the load in diode connected CML inverter by scaling the load TFET. Note that the output voltage levels have a common mode voltage. This needs to be negated in the final stage of the digital circuit being implemented.

A reduction of the load resistance value in resistive load design is found to greatly increase its operation frequency, reaching 140 MHz frequency or 0.7 ns propagation delay. Similar effects are found for using a lower resistance diode connected TFET load, implemented with parallel devices. Reduction of the supply voltage is found to greatly reduce the oscillation frequency but providing a much lower power dissipation, our initial tests achieve 80 kHz operation at only 60 nW per stage for a 0.1 V supply using 100 kΩ resistive load.

Table 3: Simulated oscillation frequency of the 5-stage CML ring oscillator for different designs / bias points, targeting power dissipation limits of 1, 10, and 100 µW per logic gate (CML inverter stage). Also presented is the corresponding propagation delay and power dissipation per a single CML inverter stage.

Load	Bias (V)	Frequency (MHz)	Inverter propag. delay (ns)	Power per inverter (uW)
Resistive (100 kΩ)	0.5	0.90	110	1.45
Resistive (1 kΩ)	0.5	140	0.7	25.8
Resistive (100 kΩ)	0.3	0.23	440	0.83
Resistive (1 kΩ)	0.3	25.0	4	7.75
Resistive (100 kΩ)	0.1	0.08	1300	0.06
Diode conn. TFET	0.5	0.90	110	9.2
PMOS active load	0.5	8.4	12	0.4

A technology cross section of the TFET device and interconnects is shown in Figure 37. The vertical nanowire TFET (source on top) is fabricated with minimal AlOx interlayers to allow rapid process runs. This inflicts a penalty in inter-electrode capacitance that limits the operation speed of the device. One stepping stone towards fast TFET logic is to integrate the devices with a more high-speed RF-type BEOL technology.

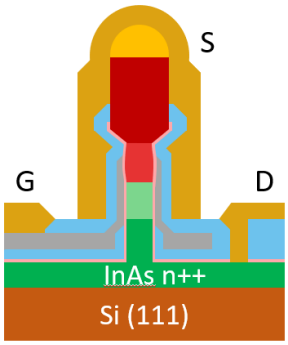


Figure 37: Technology cross section of the III-V nanowire TFET technology on Si, using simple AlOx interlayers for rapid turnaround in a technology with source-on-top nanowire design.

Layout of the TFET sample is illustrated in Figure 38. The single wire devices are placed in a large array with large pads on this DC test mask. Three adjacent devices are connected on pad-level to form the core of the TFET source coupled CML inverter and the remaining connections will be done off-chip in this version.

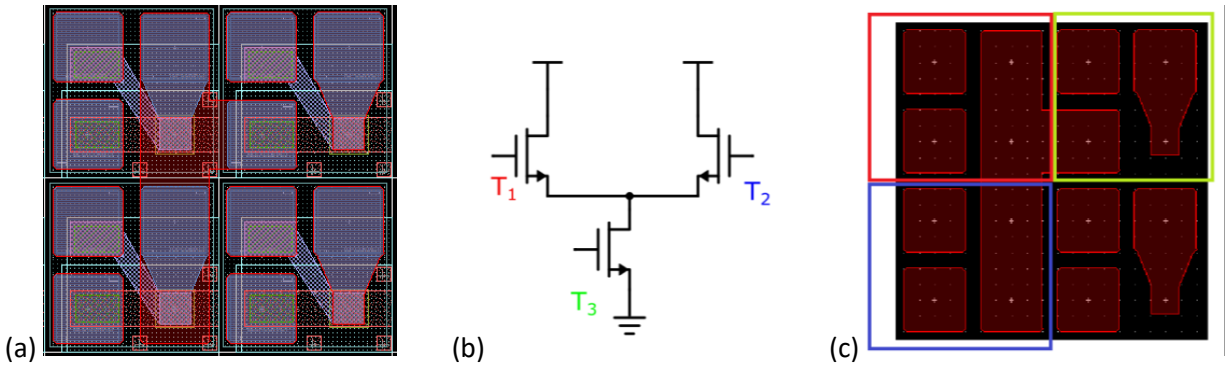


Figure 38: (a) Layout of four adjacent TFETs on the DC test mask. (b) Circuit with marked devices and (c) top-level pad connections used for the source coupled CML inverter.

FD-SOI CMOS Digital Circuits (LETI)

This subsection presents the design of a high performance Ring Oscillator (RO) at cryogenic temperatures in 28-nm FD-SOI CMOS Technology. The designed circuit has two main goals: firstly, to evaluate the oscillation frequency (gate delay) versus the temperature and secondly, to determine the most adapted temperature for future energy-efficient CMOS digital applications.

Schematic

The schematic of the Ring Oscillator (RO) is shown in Figure 39. This tunable cryogenic RO architecture consists of 4 switchable loops of 5, 7, 9 and 11 CMOS inverters. A big output buffer is added to improve RF output signal and facilitate cryogenic measurements. In the case of standard bias, the Oscillation Frequency (F_o) decrease at cryogenic temperatures from 9 GHz (300K) to 4 GHz (85K). A study of back-gate voltages to improve cryogenic digital performance [12] was done in order to use V_{TH} compensation and to observe an increase of Oscillation Frequency instead of a decrease as in the current case.

Note: The Design Kit does not provide temperature model above 70K (model in progress).

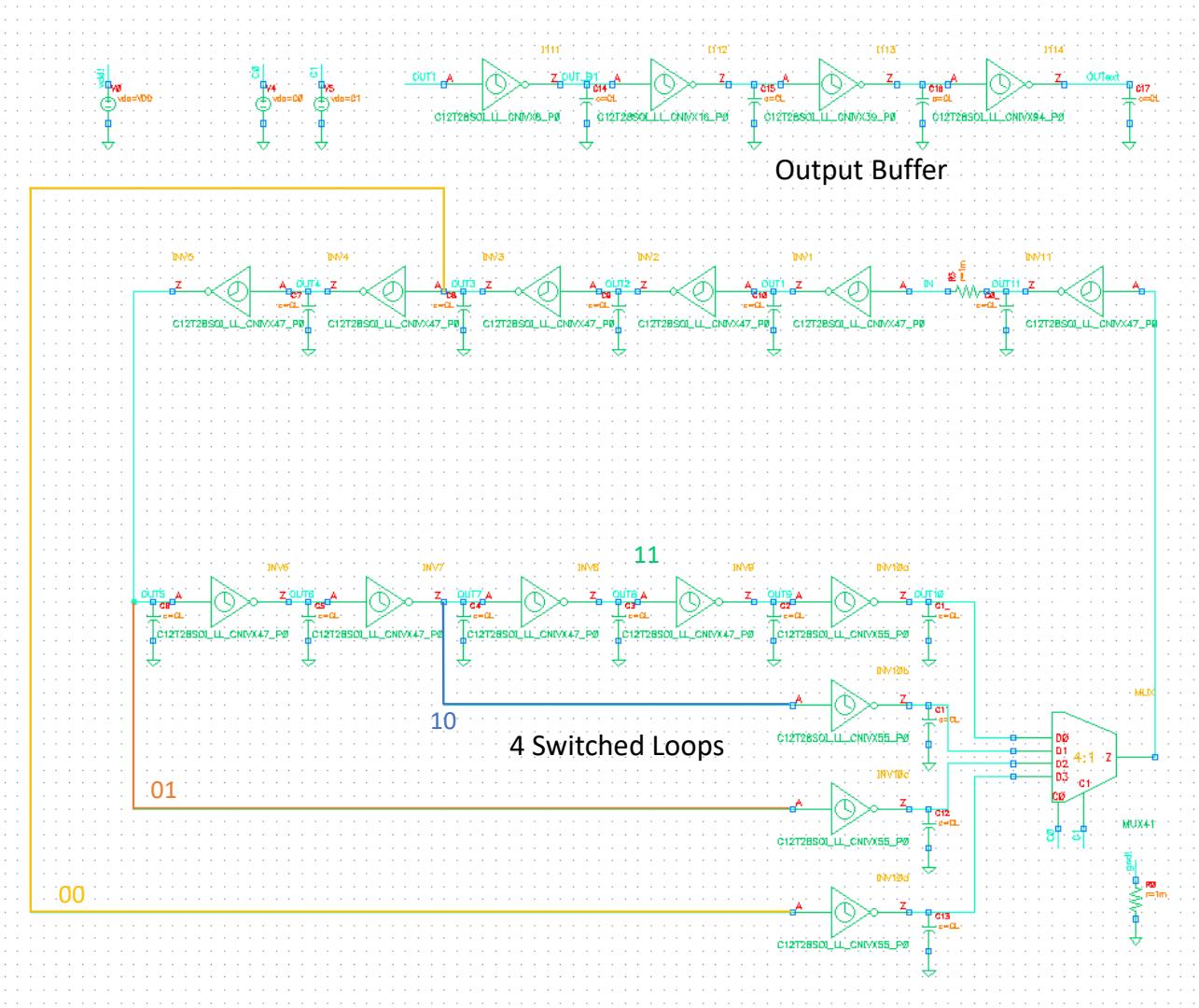


Figure 39: Schematic of the final designed tunable designed cryogenic Ring Oscillator. LVT MOSFETs: L_G = 28 nm; W_{NMOS} = 350 nm; W_{PMOS} = 550 nm.

Layout

The circuit is implemented in 28 nm FDSOI 8ML ST (STMicroelectronics) technology. Inverters use LVT transistors. The size of the finished layout is : 770 µm x 605 µm. The chip presents:

- 2 RF Signal PADs (59 µm x 45 µm) and
- 6 Supply PADs (65 µm x 65 µm).

As a first step, on-wafer probing measurements are planed at 300 K. After, a PCB will be added by Wire Bonding to allow cryogenic temperature measurements.

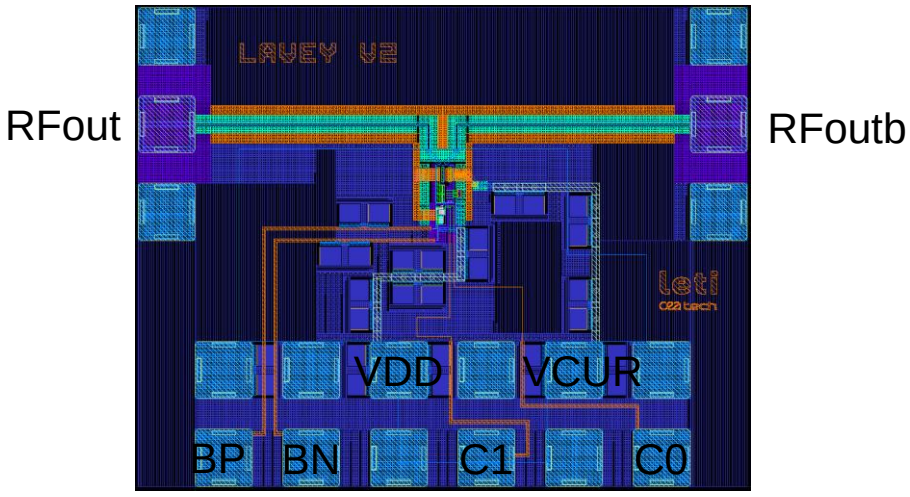


Figure 40: Layout of the tunable cryogenic RO.

Simulation Results

The RO architecture is tunable from 5 GHz up to 15 GHz (Freq. cent. = 9.33 GHz) at 300 K temperature.

The oscillation frequency of the 4 digitally switched loops are (controlled by MUX nodes C1/C0):

00 : Fc = 6.1 GHz (@300 K)

01 : Fc = 7.2 GHz (@300 K)

10 : Fc = 9.1 GHz (@300 K)

11 : Fc = 12.2 GHz (@300 K)

Between these 4 frequencies, analog tunability with VDD (and VB) allows to modify the oscillation frequency from 5 GHz up to 15 GHz.

The output buffer is differential and is controlled by VCUR.

Standard voltages: VCUR = 1 V; VDD = 1 V.

The power consumption P_{DC} is equal to 27 mW (at 300 K).

BackGates biasing addition (BN = VB, BP = -VB) allows to restore transistor performance at cryogenic temperatures as shown in Figure 41.

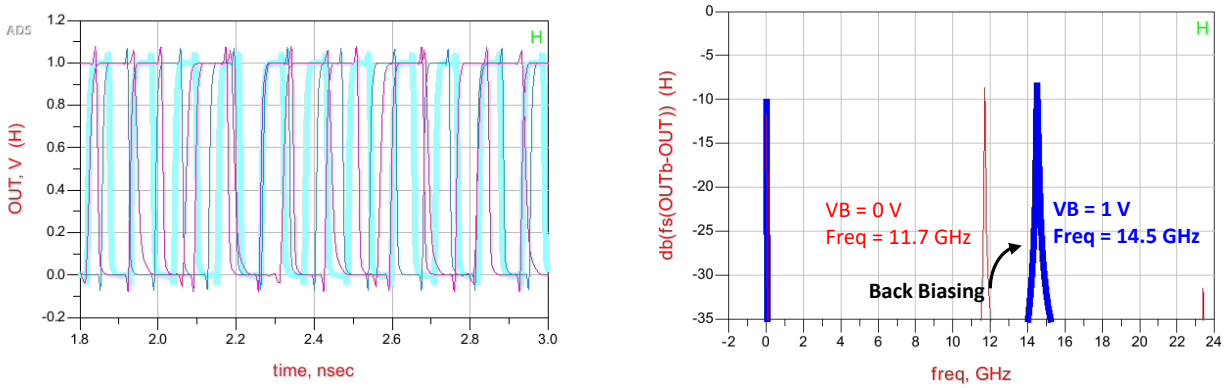


Figure 41: Simulation results of the designed cryogenic Ring Oscillator: Output Waveforms (left) and spectrum (right) 11 @200 K.

Noise Measurement System (NMS)

Recent advancements in the quantum computers have shown the need of cryogenic electronics working under extremely low noise condition with limited power budget. This has been accurately reported in the Deliverable – D3.1 *(Overview of cryogenic integrated and improved quantum computer electronics)*.

Designing at very low temperature (<4 K) presents new challenges for the engineers [13], [14] and an accurate noise model (which will be develop in WP2) is instrumental in this regard therefore, in order develop it, noise measurement data is needed.

It is clear that the devices cannot be directly probed and characterized, as their noise would be covered by the instrumentation noise floor, especially at the lowest temperature. Thus, an integrated system which can amplify the noise directly on chip is necessary. This is why EPFL is developing a Noise Measurement System (NMS) IC in order to characterize both low frequency and white noise from room- to cryogenic-temperature.

Measuring on-chip the devices white noise may prove challenging as the characterization cannot be carried out on a band wide enough to neglect the flicker noise in order to reduce the power consumption by operating at low-current and low-Gm regimes. This means that flicker noise contribution needs to be isolated effectively and one way on doing that is implementing a solution based on the chopper stabilisation principle [15]. Moreover, it is important to have a system which is able to set a proper operating point for the devices to better control the current and the transconductance on the transistors because, by a proper biasing of the MOS, the *Gm* can be controlled and kept constant whereas the current can be changed (and viceversa). This would help to distinguish, at low temperature, the shot noise (which depends on the current) and the thermal noise (which is proportional to temperature and depends on *Gm*).

The circuit shown in Figure 42 is the core of the NMS and its main purpose is to characterize the noise of the M_1 and M_2 (devices under test), and it will be implemented in 28 nm FDSOI technology. The biasing point is controlled by external voltage and current sources.

In order for the circuit to be effective in characterizing the transistors, it needs to consider the noise coming from other devices and offer the possibility to de-embed it. As shown in Figure 42, the noise coming from the DUTs (modelled as current generator) is expressed with its PSD as:

$$S_{I,M1-2} = \gamma \cdot 4kT \cdot Gm_{1,2}\left(1 + \frac{f_k}{f}\right) \quad (1)$$

where γ is the noise excessive factor which we wish to characterize at different operating regions (from weak to strong inversion), k is the Boltzmann's constant, T is the temperature, $Gm_{1,2}$ is the DUTs transconductance, f_k is the flicker corner frequency and f is the frequency.

The noise of the two OpAmp is modeled as an input referred voltage source $E_{N1,2}$ characterized as

$$S_{V,EN1-2} = S_0\left(1 + \frac{f_k}{f}\right) \tag{2}$$

where S_0 is the equivalent input referred white noise of the OpAmp.

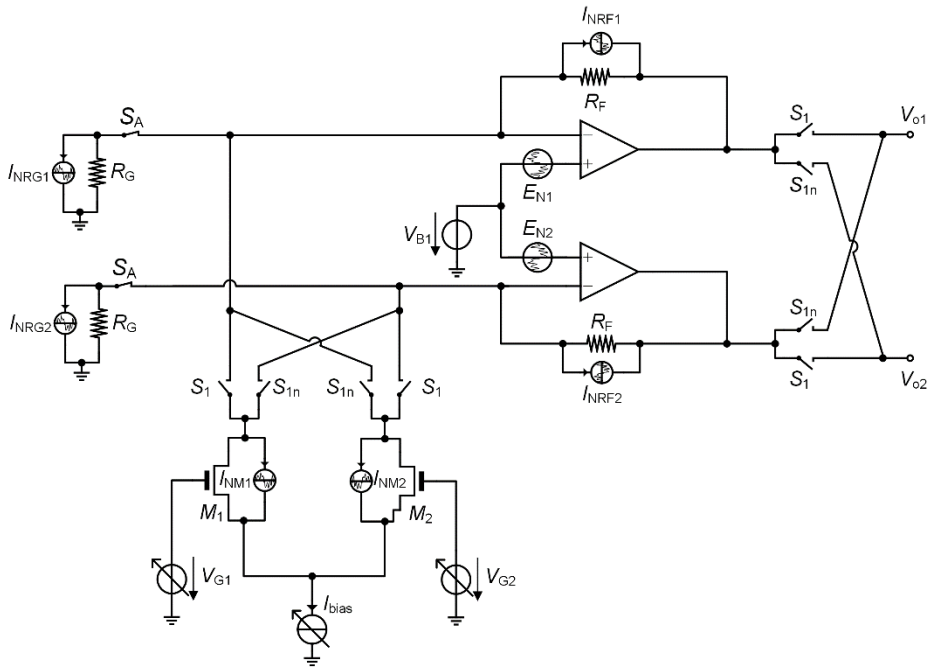


Figure 42: Noise measurement system full implementation.

The noise of the resistors is modeled as a current source defined with its PSD as:

$$S_{I,R} = \frac{4kT}{R} \tag{3}$$

The circuit in Figure 42 is used in different configuration, according to which switches are closed, open and toggled by an external clock. In the next sections three different configurations are shown: the first one used to evaluate only the white noise of the input pair, the second one to evaluate the white and flicker noise from the OpAmps and the third one to evaluate the DUTs flicker noise.

DUTs White Noise Evaluation

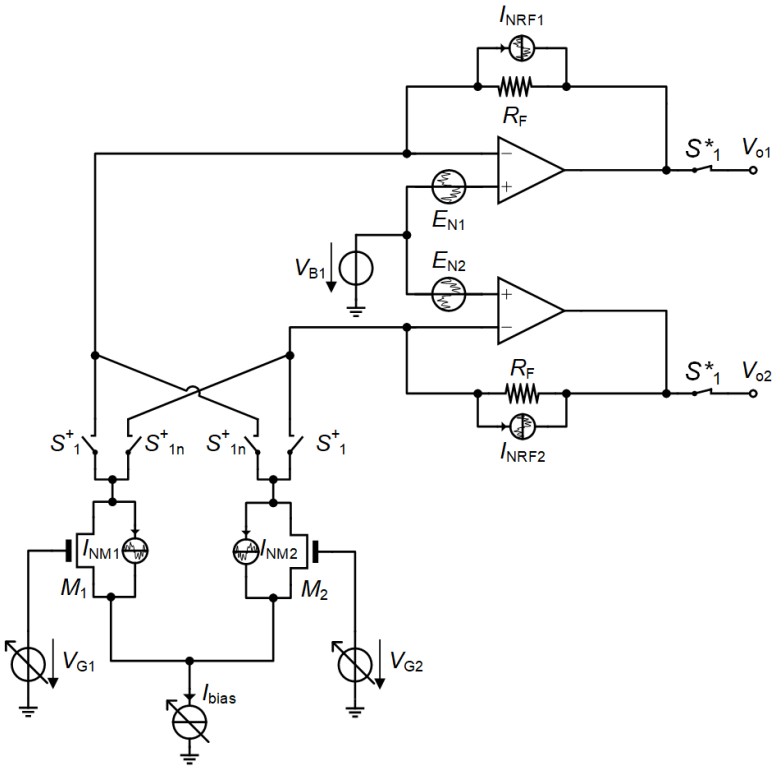


Figure 43: Noise configuration system: configuration to evaluate the DUTs white noise.

Figure 43 shows the configuration used to evaluate the DUTs white noise. With respect to the circuit in Figure 42, the switches S_A are open, the switches on top of the MOSs toggle thanks to an external clock and only the pair S_1 is closed at the output of the OpAmps. This means that the noise current coming from M_1 and M_2 is modulated by a square wave of frequency f_{chop}. The modulated noise current is calculated as [15]:

$$S_{I,M1-2,mod} = \left(\frac{2}{\pi}\right)^2 \sum_{n=-\infty,\ n\ odd}^{+\infty} \frac{1}{n^2}\ S_{I,M1-2}\left(f - n \cdot f_{chop}\right) \approx S_{n0,M}\left(1 + \frac{17 f_k}{2\pi^2 f_{chop}}\right) \qquad (4)$$

where f_k is the corner frequency and $S_{n0,M}$ is the PSD of the white noise. If $f_k = f_{chop}$ then the terms in parenthesis is about 1.86.

The effect of the modulation can be seen in Figure 44, where the blue line represents the DUTs noise current and the orange line the modulated noise current. The plot is normalized to the chopping frequency (which in this case has been set equal to the corner frequency) and to the gain (in order to have the white noise equal to 1). It can be observed that the modulation shifts the low frequency component around the odd harmonics of the square wave driving the switches, leaving a flat signal around DC whose amplitude is equal to the white noise value multiplied by 1.86.

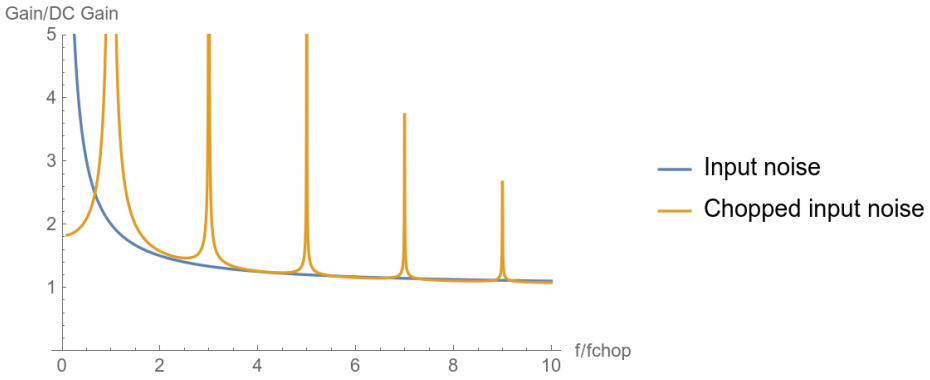


Figure 44: Effect of the modulation on the noise current.

The modulated current is then amplified by the transimpedance amplifier composed by the OpAmp and R_F, which sets also the DC voltage at the transistor drains to V_{BIAS} thanks to the virtual ground principle.

It could be noticed that the noise coming from R_F and the modulated current have the same transfer function to the output whereas the noise of the OpAmps directly transfers to the output. Therefore, it is key to know precisely the contributions from the resistor and the OpAmp to de-embed them. For the former it suffices to know the resistance value whereas for the latter a dedicated structure is necessary and it is described in the next Section.

OpAmp Noise Evaluation

As mention in Section 0, it is pivotal to evaluate and characterize the noise coming from the OpAmp, both white and flicker noise. For this purpose, the circuits in Figure 45 are used, in particular (a) is used to evaluate the white noise by modulating the output and (b) is used to evaluate the 1/*f* noise.

With respect to the circuit in Figure, the switches S_A are closed whereas the switches on top of the DUTs are open. The switches at the output are either toggled or one pair is closed and the other one is open as shown respectively in Figure 45(a) and (b). In both cases the configuration composed by the OpAmp, R_F and R_G implements a non-inverting amplifier which amplifies the OpAmp noise, modelled as an equivalent voltage source at the positive input, ideally by a factor $1+R_F/R_G$. The noise current from R_F and R_G are directly transferred to voltage output multiplied a factor R_F.

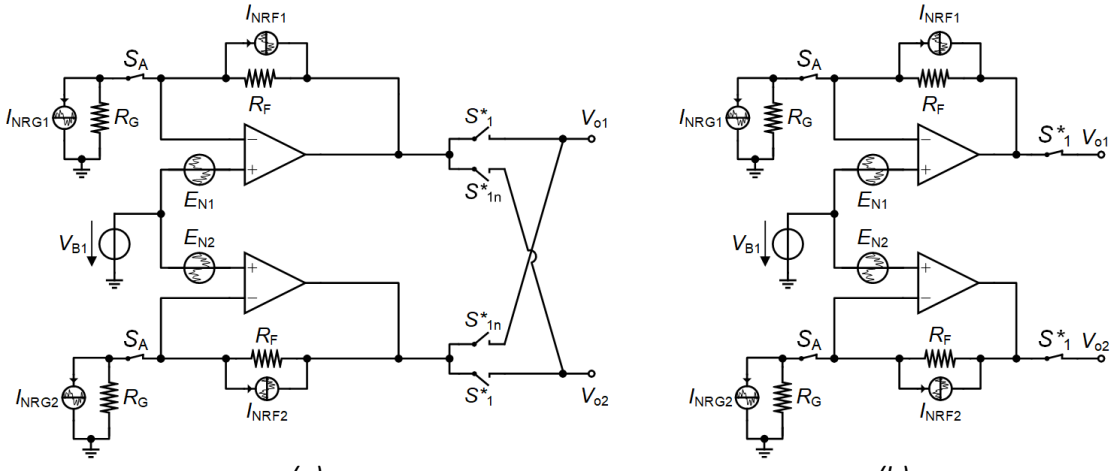


Figure 45: Configuration for the OpAmp noise evaluation. (a) is used to evaluate the white noise by modulating the output (b) is used to evaluate the 1/f noise.

The result from the configuration in Figure 45(a) is similar to what shown in Figure 44 as the low-frequency components are pushed around the odd harmonics of the modulating square wave and this allows evaluating the OpAmp amplified white noise. On the other hand, the configuration in Figure 45(b) is used to characterize the amplified 1/*f* noise by simply reading the output. Also, in this case it is important to know the resistors value in order to know the amplification factor and to de-embed their noise contribution.

DUTs Flicker Noise Evaluation

Figure 46 shows the configuration used to evaluate the DUTs flicker noise. This circuit implements a full chopper amplifier [15] where only the low frequency component of the OpAmps are pushed at higher frequency, as they are modulated only once whereas the current coming from the DUTs is modulate and then demodulated at the output in order to restore it.

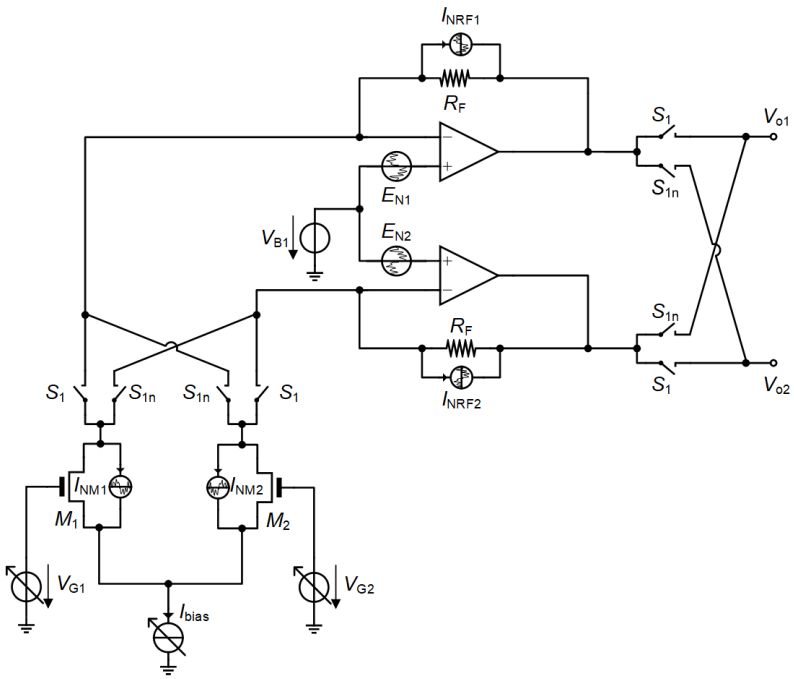


Figure 46: Noise configuration system: configuration to evaluate the DUTs flicker noise.

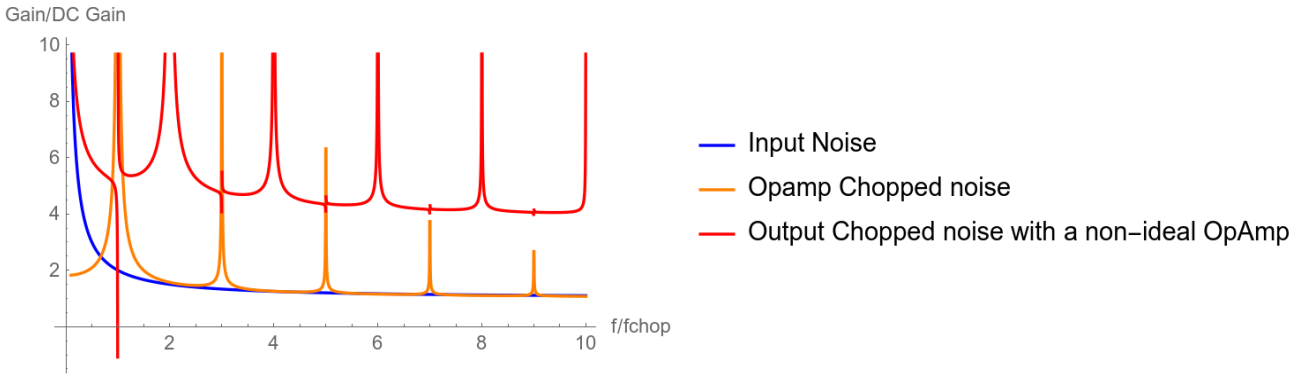


Figure 47: Effect of the chopping stabilization.

Figure 47 shows the effect of the chopping amplifier in a normalized plot similar to the one shown in Figure 44. The blue line represents the noise of the DUTs, the orange line represents the chopped noise of the amplifier and the red line is the DUTs noise after amplification and demodulation. In this case also a non-ideal OpAmp has been considered, modelled with limited gain and a one-pole characteristic. It can be noticed that,

especially due to the limited bandwidth, the de-modulation is not perfect but has some folding around the even-order harmonics of the chopping frequency. This is not critical as long as the $1/f$ characteristic can be evaluated up to the chopping frequency, which can set exactly equal to the corner frequency.

Conclusion and Future Outlook

A noise measurement system has been presented whose main objectives are to characterize the transistor white noise (with the purpose to distinguish between shot and thermal noise) and flicker noise, from cryogenic to room temperature. The system will allow to amplify on chip the noise coming from the devices and to de-embed the contributions coming from other noise sources thanks to the chopping technique.

The circuit will be implemented in 22 nm FDSOI technology and the next steps are system level characterization with CAD tools in order to validate this analysis. The tape-out is expected to be late July. The obtained results will then help to develop a cryogenic noise model in WP2.

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