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1 Introduction

The objectives of WP2 are i) to perform a detailed LF and RF electrical characterization and parameter extraction of the device operated under deep cryogenic conditions, and, ii) to develop associated LF and RF analytical compact device models valid at very low temperature and usable in circuit design simulation platforms. More specifically, Task 2 and Task 4 of WP2 aim at providing i) basic electrical characterization and improved parameter extraction, ii) insights into carrier transport properties (mobility, velocity) at very low temperature under degenerate statistics conditions for various devices (Si vs III-V) and iii) DC and RF electrical characterization of device operation at extremely low temperatures (20mK-4K) for physical understanding of device operation under deep cryogenic conditions for various Si and III-V devices.

The deliverable D2.7 due at M30 reports on the last campaign of electrical measurements made for electrical parameter, interface dielectric trap and RF (S parameter and NF) characterization on devices coming from various technologies operated at cryogenic condition such as 28nm Si FDSOI from industrial platforms as well as on III-V MOSFETs, III-V HEMTs, TFETs and NW MOS devices developed in WP1 consortium.

2 In-depth electrical characterization of deca-nanometer InGaAs MOSFET down to deep cryogenic temperatures (contributor: INPG/IBM)

2.1 Introduction

As the research on quantum computing (QC) advances, the need for active electronic devices that operate at deep cryogenic conditions will increase. This necessity is better understood when considering the qubit readout electronics [2.1]. While it is currently an open question how many qubits cryogenic Si CMOS circuits will be able to support, other device technologies, such as III-Vs, may in the future be better suited. Thanks to their enhanced mobility, III-V MOS devices can provide the same ON current at lower power supply voltages, and by turn reduced power consumption and heat dissipation, crucial at QC operation temperature. [2.1] Thus, the precise identification of their electrical parameters' behavior with temperature and channel length is required for reliable modeling and circuit design. On the other hand, as this technology is not as mature as its Silicon-based counterparts (Bulk, FDSOI, and FinFETs), the need of full electrical characterization down to deep cryotemperatures, becomes challenging and critical, particularly in view of the emerging technology of QC.

To date, Si CMOS has been extensively studied including at cryogenic temperatures [2.1-2.6]. Similar studies on InGaAs MOSFETs are currently lacking. Therefore, in this work, we study scaled InGaAs MOSFET devices down to cryogenic temperatures, to determine their temperature- and size-dependent properties and compare them with Si CMOS. In particular, we compare the physical limits of the subthreshold swing at cryogenic temperatures. Finally, key cryogenic device properties are benchmarked with Si CMOS. The work provides valuable understanding of the cryogenic operation of III-V MOSFETs, and the results indicate that these devices are highly promising for cryogenic low-power quantum computer applications.

2.2 Device under test

The devices under test were fabricated by IBM Zurich within WP1 [2.7], based on a III-V on insulator tehnology, incorporating a 20 nm InGaAs film, insulated by a buried oxied and integrated on Silicon substrates through direct wafer bonding (Fig.2.1). The fabrication process is CMOS-like with replacement metal gate, raised source/drain regrowth and a high-k metal gate. The devices share a common gate width value of W = 1 μm and channel lengths spanning from L = 300 down to 10 nm. Fig. 2.1 also shows a TEM image of a L = 10 nm device. Henceforth, we will refer to the nominal value. The measurements were carried out at wafer level down to 10K using a HP 4155A parameter analyzer and a SussTech 300mm Cryo probe station.

In order to extract the main parameters that define the MOSFET performance, we utilized the Y-function method, expressed through $Y(V_g) = I_d/\sqrt{g_m} \approx \sqrt{\beta}(V_g - V_{th})$ [2.8], where $\beta = W\mu_0 C_{ox} V_d / L$. This function suppresses any access resistance effect and thanks to its linear behavior versus V_g at strong inversion, the linear fit can provide the threshold voltage, V_{th}, as well as the low-field mobility, μ_0, value through the x-axis intercept and slope, respectively.

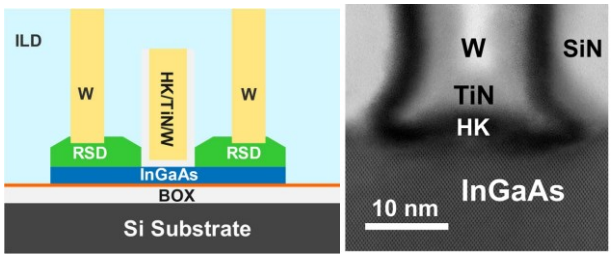


Fig.2.1 *(Left) Schematics of studied III-V MOSFETs. (Right) TEM image of a device with nominal 10 nm gate length. Courtesy of IBM Zurich.*

2.3 DC MOSFET parameter extraction

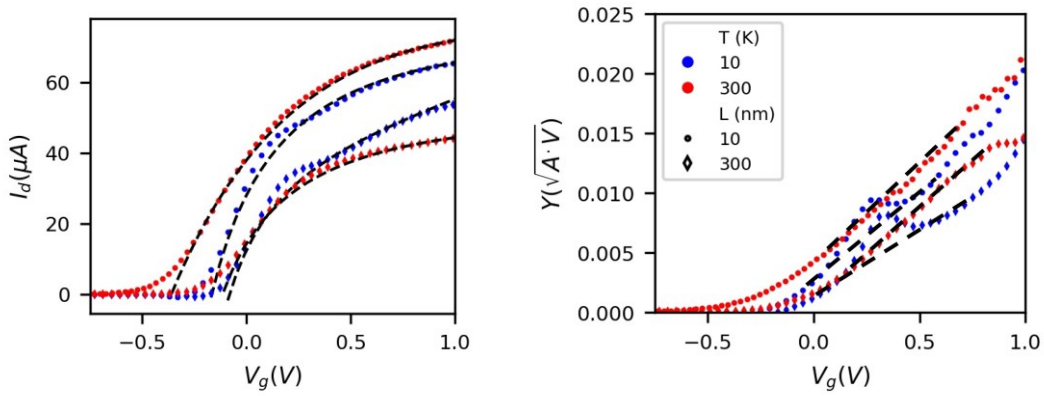
2.3.1 Preliminary observations

The measured I_d -V_g input characteristics in linear regime are plotted in Fig. 2.2a, for the two temperature limits (10 K and 300 K). Through a first glance, we can already observe how the threshold voltage, V_{th}, is affected by both channel length and temperature: on one hand, for a shorter channel V_{th} shifts downwards ("V_{th} roll-off" short channel effect), while on the other hand, it increases for a decreasing temperature.

Moreover, we can notice some kind of a shoulder/hump in the high V_g region, in both the I_d-V_g and the Y-V_g (Fig. 2.2b) curves: this effect is most likely to be related to the onset of conduction in the L valley [2.9] of III-V. What is most important for our study, however, is that this hump does not impact the overall linear behavior of the Y function in strong inversion, allowing us therefore an easy and reliable extraction of the main operation parameters.

2.3.2 Analysis of extracted parameters in linear region

When going down to low temperatures (LT), several effects are taking place. First, due to the Boltzmann statistics, as the temperature decreases, fewer and fewer electrons are promoted to the conduction band for the same gate voltage. This is reflected in an increase in threshold voltage as going towards lower temperatures, as shown in the extracted V_{th} values, plotted versus temperature for all measured gate lengths in Fig. 2.3. This increase at low temperatures reaches a maximum V_{th} value, which corresponds to the degenerated behavior of the semiconductor at that range of temperatures [2.10].



(a) (b)

Fig. 2.2. *Drain current (a) and Y-function (b) versus gate voltage at V_d = 30 mV for L = 10 and 300 nm at T = 10 and 300K. The dashed lines represent the fitting of the plots, based on Y function and linear regression respectively.*

Moreover, the transition between OFF and ON states becomes sharper (Fig. 2.4), yielding a consequent decrease of the subthreshold swing, SW, for low temperatures, down to a settling value of about 10 mV/dec, which is attributed to the exponential band tails of states [2.3]. This behaviour of SW is confirmed for the measured III-V devices, as shown in Fig. 2.5, where the extracted values of SW are plotted versus temperature for certain channel lengths. Conversely, as the temperature lowers, there is less and less vibrational energy in the lattice, causing a decrease in phonon scattering , which allows an increase in the low-field mobility, $\mu_{0,}$ as shown in a, where the extracted values of μ_0 are plotted versus temperature for all measured gate channel length. This increase is evidently more pronounced in longer channel devices, whereas, in shorter channels, defect (neutral impurity) scattering is prevailing due to source/drain regions proximity, yielding a generally lower mobility and also a less significant increase at lower temperatures [2.6]. As it can be shown through Poisson-Schrodinger simulations [2.9], the effect of L valley carrier population becomes only visible below 100K, giving rise to specific structure in I_d-V_g and Y-V_g characteristics (Fig. 2.2).

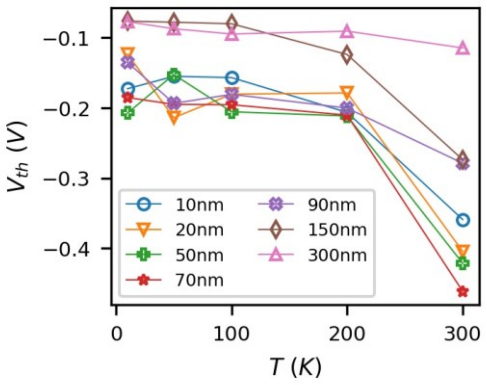


Fig. 2.3. *Extracted threshold voltage versus temperature for V_d=30mV for various channel lengths.*

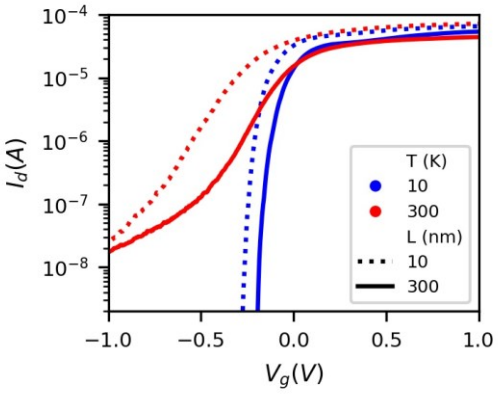


Fig. 2.4. *Drain current versus gate voltage at V_d=30mV for L =10 and 300 nm at T= 10K and 300K.*

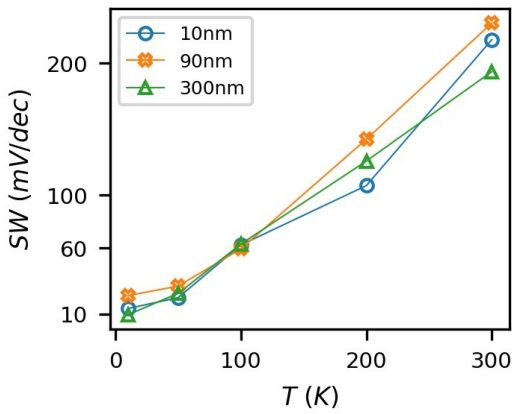


Fig. 2.5. *Extracted subthreshold swing at V_d=30mV versus temperature for different lengths from 10 to 300 nm.*

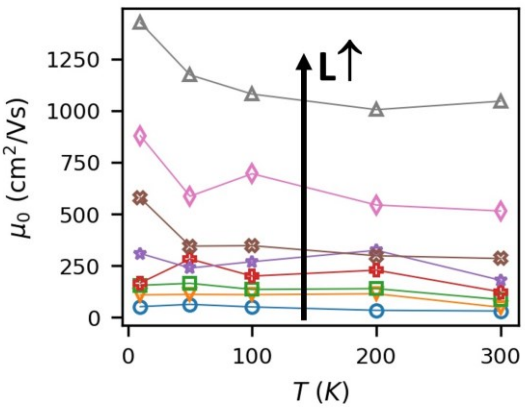


Fig. 2.6*. Extracted low-field mobility at V_d=30mV versus temperature for different lengths from 10 to 300 nm.*

2.3.3 Behavior in saturation region

As we proceed towards the analysis of the device parameters in saturation region of operation (V_d=1V), we observe that both 10 and 300 nm length devices, plotted in Fig. 2.7, show no significant variation in the ON region as going to low temperatures, except for an increased Vt in the 10 nm at 10K. On the contrary, we notice that in saturation region, the curvature created by the takeover of L valley is no longer visible at low temperature. This can be explained when considering that the drain current is obtained by integration along the channel from source to drain [2.11]: close to the drain region the influence of high V_d does not allow the quasi Fermi level to fill the L valley, thus attenuating its effect. When extracting the μ_0 values through Y function, plotted in Fig. 2.8, compared to the linear region, the devices present a μ_0 reduction due to velocity saturation (v_{sat}) effect [2.4]. Moreover, it is worth noticing how the extracted mobility never reaches the ballistic limit [2.5], revealing that the exponential behaviour of μ_0 with respect to channel length is in fact scattering-related. The extracted values of v_{sat} in saturation region are plotted in Fig. 2.9, showing a good stability with respect to temperature and a slight increase for a decreasing channel length due to overshoot effect.

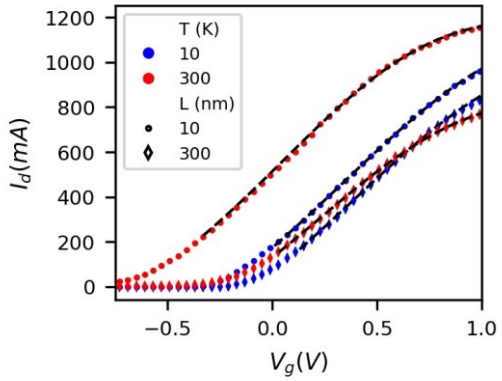


Fig. 2.7. *Drain current versus gate voltage at V_d=1V for L = 10 and 300 nm at T = 10 and 300K. The dashed line shows the fit reconstructed with the parameters extracted by Y function.*

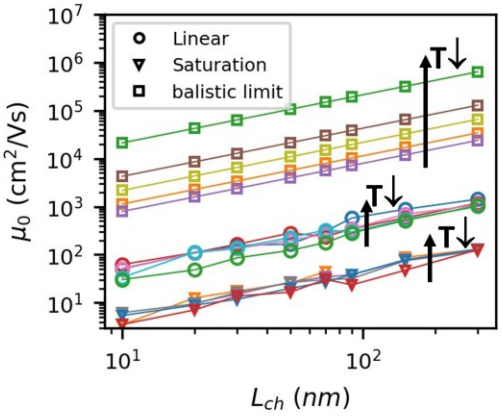


Fig. 2.8. *Extracted low-field mobility versus channel length for linear and saturation regions along with theoretical ballistic limit.*

2.3.4 Benchmarking III-V against Si for cryogenic condition

Fig. 2.10 illustrates the extracted parameters of μ_0, SW and v_{sat} along with respective extractions done for Si [2.6] channel Fully Depleted (FD) SOI MOSFETs. When comparing the III-V MOSFET devices to this more mature technology like industrial FDSOI (Fig. 2.10) [2.6], we note that although SW is much higher for III-V at 300K, both technologies reach the lowest limit value at 10K. Moreover, despite the higher interface trap density at the Al_2O_3 interface, III-V shows higher μ_0 and v_{sat} at all temperatures, revealing a great III-V potential for cryo-related applications with further technology developments and the chance to over perform Si FDSOI in certain cases.

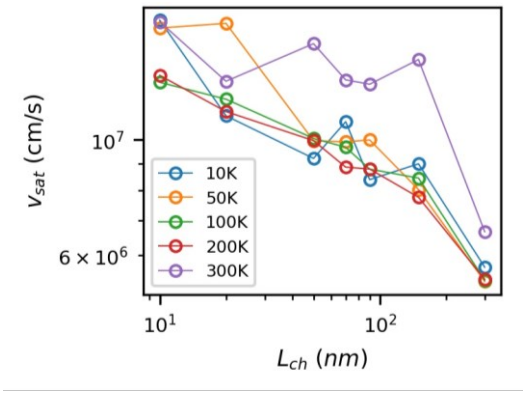


Fig. 2.9. *Extracted saturation velocity versus channel length for various temperatures.*

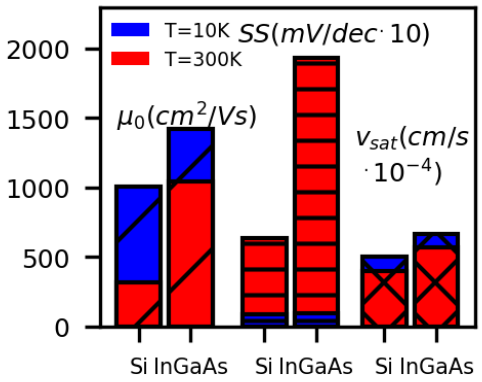


Fig. 2.10*. Comparison of extracted parameters between III-V and Si [2.5].*

2.4 LF noise performance

The low frequency noise has been measured versus frequency (4Hz-100kHz) in such InGaAs MOSFETs with dimensions W=5µm and L=120nm or 300nm using the NOISYS system [2.12] at wafer level on a 200mm Susstec cryostation between 10K and 300K. Typical 1/f drain current S_{Id} spectra obtained at 10K and 300K are shown in Fig. 2.11 for various gate voltages varying from weak to strong inversion. The normalized drain current noise S_{Id}/I_d^2 has then been extracted for a fixed frequency (f=10Hz). These data have been well fitted (see Fig. 2.12) using the carrier number fluctuation (CNF) model [2.13],

$$\frac{S_{Id}}{Id^2} = S_{Vfb}\left(\frac{gm}{Id}\right)^2 \tag{2.1}$$

where $S_{Vfb}=q^2.\lambda.kT.Nt/(W.L.C_{ox}^2.f)$ is the flat band voltage spectral density related to the slow oxide states (border traps) volume density N_t, with λ being the tunneling constant in the dielectric (≈0.1nm). The slow oxide trap volume density N_t has been extracted as a function of temperature and is shown in Fig. 2.13. As can be seen, N_t is found always larger than 10^{20}/eVcm^3, which is typically one to two orders of magnitude higher than in 22nmFDSOI MOS devices [2.14].

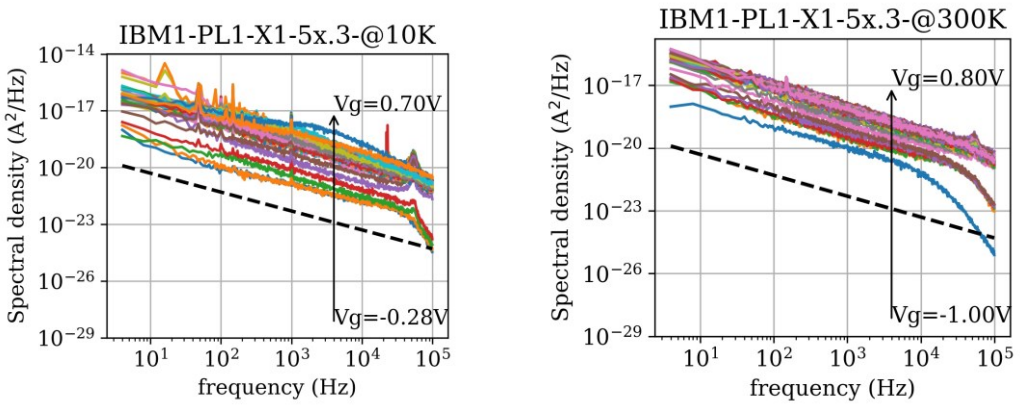


Fig. 2.11. *Drain current spectral density S_{Id} versus frequency f obtained on InGaAs MOSFETs for various gate voltages (W=5µm, L=300nm, V_d=30mV).*

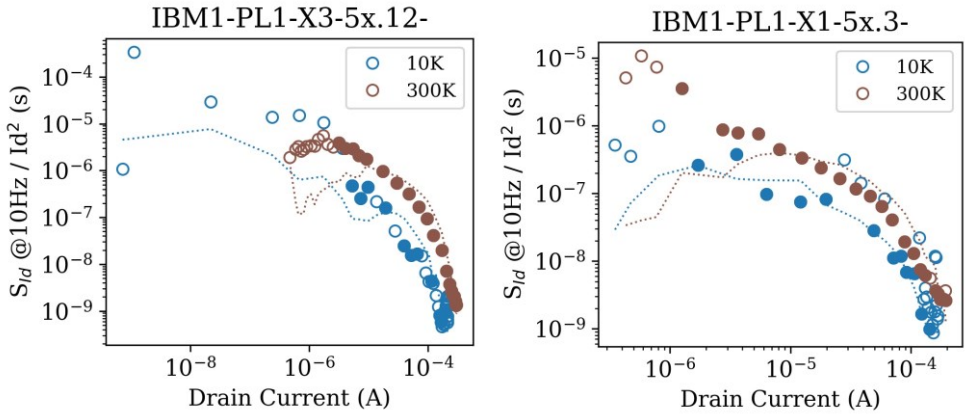


Fig.2.12. *Normalized drain current noise S_{Id}/I_d^2 versus drain current I_d (symbols) obtained on InGaAs MOSFET for T=10K and 300K and L=120nm and L=300nm (V_d=30mV, f=10Hz)). The dotted lines show the fitting done with CNF model.*

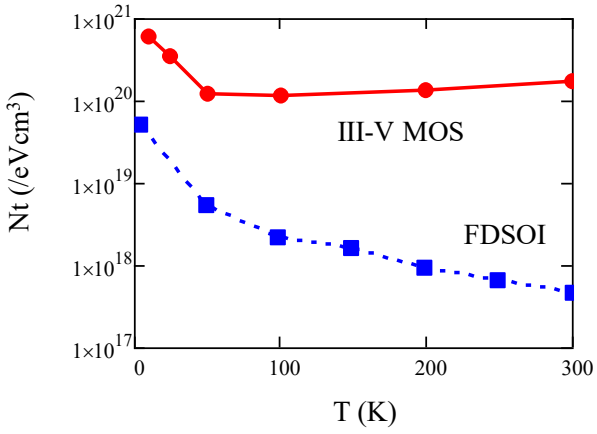


Fig.2.13. *Temperature dependence of slow oxide trap density N_t obtained on InGaAs MOSFET. Results for 22nm FDSOI MOS devices are also shown for comparison [2.14].*

3 Cryogenic electrical characterization of 200mm CMOS compatible GaN/Si HEMTs (Contributor: INPG/LETI)

3.1 Introduction

Cryogenic power electronics is a key enabling technology for various applications such as electromechanical drives, transportation, renewable systems and power networks [3.1-3.2]. It will bring higher power density, higher efficiency and superior performances due to higher operation speed, lower power dissipation stemming from reduced voltage, better switching characteristics, shorter transmission times due to lower metal resistance, increased integration density, better digital and analog device/circuit performances [3.1-3.2]. In this context, GaN HEMT technology has emerged as a promising candidate in cryogenic power electronics for high frequency and high power microwave applications due their high two dimensional electron gas (2DEG) mobility as operated at very low temperatures [3.3-3.9]. However, although several studies have already been reported about the cryogenic performances of GaN HEMT devices [3.10-3.13], there is still a lack of detailed analysis of the electronic properties of the channel and access regions under cryogenic operations.

Therefore, in this work, we present, for the first time, a complete electrical characterization of the GaN HEMT transistor MOSFET parameters (mobility, threshold voltage, subthreshold swing, source-drain resistance…) as a function of gate length and gate-source/drain distance operated down to deep cryogenic temperatures. We demonstrate that the 2DEG mobility is enhanced by phonon scattering reduction, as well as the switching behaviour considerably improved at very low temperatures. Moreover, we show that the access region resistance strongly limits the on-current at high gate voltage.

3.2 Experimental details

The HEMT devices under investigation belong to a GaN technology processed on 200 mm Silicon wafer designed for high frequency applications [3.14]. Fig. 3.1 illustrates the device structure and cross section. The epitaxial stack was grown using metal organic vapor phase epitaxy (MOVPE) on a 200 mm high resistivity silicon (111) substrate. The structure consists in transition layers and a 1.5 µm GaN carbon doped buffer layer followed by an AlGaN back barrier (300 nm) and a 150 nm unintentionally doped (UID) GaN channel. An AlN spacer (1 nm) and a thin $Al_{0.28}Ga_{0.72}N$ (7 nm) layer formed the barrier. A capping layer of 10 nm in situ SiN was used for passivation. Ohmic contact formation began with passivation and AlGaN barrier etching before Ti/Al deposition, chemical mechanical polishing (CMP) and annealing at 590 °C. Gate feet were patterned by ebeam lithography followed by passivation etching, TiN/W deposition and CMP. The gate head was formed by Ti/TiN/Al/TiN deposition and dry etching. Finally, vias were opened through the SiO_2 passivation and 1.4 µm Al deposition followed by lithography and dry etching formed the first level of interconnection. The test structure device gate length varies between Lg= 0.1µm up to 3µm, the source-gate length Lgs=1µm or 5.5µm, the drain-gate length Lgd=1.5µm or 5.5µm. The device gate width is Wg=100µm or 125µm.

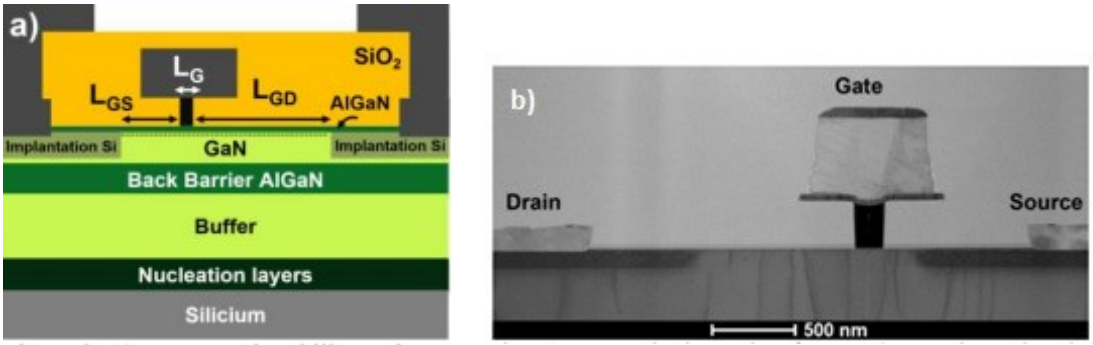


Fig. 3.1. *Schematic of epitaxial stack and TEM cross section of GaN HEMTs.*

The I_d-V_g transfer characteristics were measured in linear (V_d=50mV) and saturation (V_d=5V) regions using an HP 4156B semiconductor parameter analyser. The gate-to-channel capacitance was measured at room temperature with an HP 4284 LCR meter at a frequency of 1MHz, providing a maximum capacitance of about 1.8µF/cm^2 above threshold. The cryogenic measurements were performed on a 200mm liquid helium Susstec cryo-probe station with temperatures varying between 10K and 300K.

The MOSFET parameter extraction was carried out, on one hand, using the Y-function method, originally developed for Si MOS transistors [3.15] and recently validated on HEMT GaN devices at 300K [3.16], and, which allows removing the influence of the source-drain series resistance. The Y-function is defined from drain current I_d and transconductance g_m by [3.15],

$$Y(V_g) = I_d/\sqrt{g_m} \approx \sqrt{\frac{W_g}{L_g}.C_{ox}.\mu_0.V_d}.(V_g - V_{th}), \tag{3.1}$$

where C_{ox} is the maximum gate-to-channel capacitance associated to the coupling capacitance between the metal gate and GaN 2DEG through the AlGaN layer, μ_0 is low field mobility and V_{th} the threshold voltage. The source-drain series resistance R_{sd} is then extracted, in linear operation, from the plateau of the quantity defined below plotted at strong inversion,

$$R_{sd} = \frac{V_d}{I_d} - \frac{L_g}{W_g.C_{ox}.\mu_0.(V_g - V_{th})}. \tag{3.2}$$

On the other hand, the MOSFET parameter extraction can also be performed using the Lambert-W function modelling approach developed for Si MOS transistors at 300K [3.17] and recently extended at cryogenic temperatures [3.18]. In this case, the drain current in linear region including the R_{sd} influence is given by,

$$I_d = \frac{\frac{W_g}{L_g}\mu_0.Q_i.V_d}{1+R_{sd}.\frac{W_g}{L_g}\mu_0.Q_i}. \tag{3.3}$$

where the inversion charge Q_i is modelled from weak to strong inversion as,

$$Q_i = C_{ox}.\frac{n.kT}{q}.LW(e^{\frac{V_g - V_{th}}{n.kT/q}}), \tag{3.4}$$

where kT/q is the thermal voltage, n the subthreshold ideality factor and LW is the Lambert-W function [3.17]. This LW method presents the advantage to extract the MOSFET parameters over the full gate voltage range below and above threshold.

Finally, the Y-function method has been applied to the saturation region for the extraction of the carrier saturation velocity v_{sat} as was originally demonstrated in Si MOSFETs [3.19]. In this case, Eq. (3.1) is used to extract from the slope of the linear trend of Y(Vg) characteristics measured in saturation, the mobility degraded by the longitudinal electric field V_d/L_g, $\mu_{0d}=\mu_0/(1+\mu_0 V_d/(v_{sat}L_g))$, such that the saturation velocity can be obtained from [3.19],

$$v_{sat} = \frac{\mu_0 V_d}{L_g\left(\frac{\mu_0}{\mu_{0d}}-1\right)} \ . \tag{3.5}$$

For comparison purpose, the saturation velocity has also been extracted using the standard method based on the saturation drain current I_{dsat} and inversion charge at source terminal and given by [3.19],

$$v_{sat} = \frac{I_{dsat}}{W_g.C_{ox}.(V_g-V_{th}-R_s.I_{dsat})} \ , \tag{3.6}$$

where R_s is the source series resistance.

3.3 Results and discussion

3.3.1 Transfer characteristics

Typical drain and source current transfer characteristics I_d-I_s-V_g measured in linear region (V_d=50mV) obtained on GaN HEMT devices with a gate length of L_g=150nm at various temperatures (10K-300K) are shown in Fig. 3.2. As can be seen from the figure, there is a strong gate leakage I_g for high gate voltage in such Schottky gate devices. Indeed, the drain current I_d strongly differs from the source current I_s for V_g>1.5V. For this reason, the MOSFET parameter extraction has been restricted to V_g up to 1V in order to avoid any gate leakage influence. Nonetheless, note that the I_d-V_g curves exhibit a very good behaviour below threshold as the temperature is lowered with an improved subthreshold slope, specific of cryogenic operation. Note also that the I_d-V_g curves are saturating well above threshold due to the strong impact of the series resistance effect caused by the access regions. The corresponding transconductance g_m-V_g and Y-function Y-V_g characteristics up to V_g=1V are shown in Fig. 3.3, illustrating the increase of the maximum transconductance with temperature lowering and the linear behaviour of Y-function well above threshold.

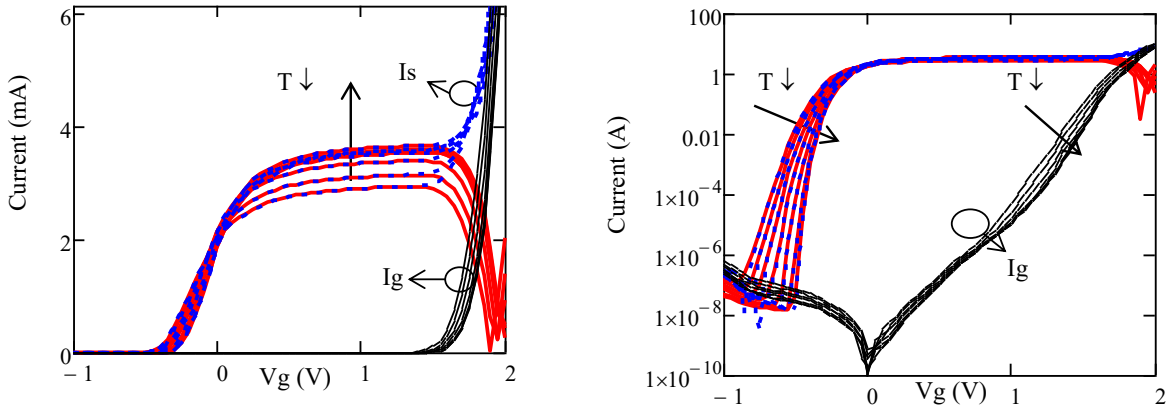


Fig. 3.2. *Typical I_d-V_g characteristics in linear (left) and log (right) scale as obtained on GaN HEMT devices for various temperatures T(K)=10, 50, 100, 150, 200, 250, 300 (V_d=50mV, L_g=150nm,*

W_g=100µm).

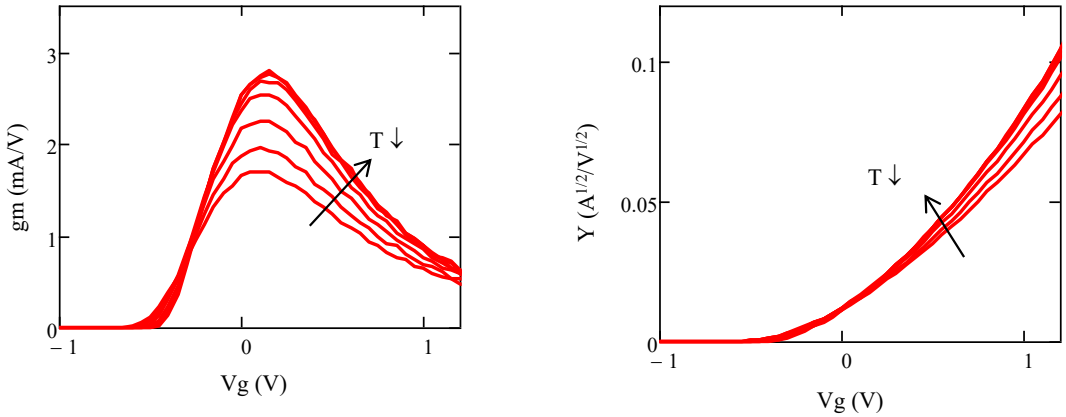


Fig. 3.3. *Typical g_m-V_g (left) and Y-V_g (right) characteristics as obtained on GaN HEMT devices with various temperatures* T(K)=10, 50, 100, 150, 200, 250, 300 *(V_d=50mV, L_g=3000nm, W_g=100µm).*

3.3.2 Y-function based MOSFET parameter extraction

Based on Eq. (3.1), the threshold V_{th} and low field mobility μ_0 were extracted respectively from the x-axis intercept and slope of the Y-function linear trends above threshold [3.15], for each gate length and temperature. Fig. 3.4 shows the variations with temperature of the obtained threshold voltage V_{th} and low field mobility μ_0 for various gate lengths. As expected from cryogenic operation, one observes a linear increase of V_{th} with temperature lowering due to carrier statistics evolution. Note also that the V_{th} roll-off versus gate length is nearly independent of temperature as mainly arising from electrostatic-induced short channel effect as is usually observed in Si MOSFETs [3.20]. Moreover, the low field mobility μ_0 is also increasing with temperature reduction due to phonon scattering diminution, especially for long channel devices, where μ_0 improves from 2000cm^2/Vs up to 4000cm^2/Vs for L_g=3000nm. It should be mentioned that these mobility values are in good agreement with literature results obtained on GaN HEMTs by Hall effect or FET parameter extraction [3.10, 3.21], pointing out the good quality of our GaN technological process. In Fig. 3.4b are also reported, for comparison purpose, the variations with temperature of the maximum field effect mobility deduced from the maximum transconductance and defined as $\mu_{femax}=g_{mmax}.L_g/(W_g.C_{ox}.V_d)$ [3.22], clearly revealing the huge underestimation of the mobility values obtained using this method, which is indeed inappropriate in the presence of large R_{sd} effect [3.23].

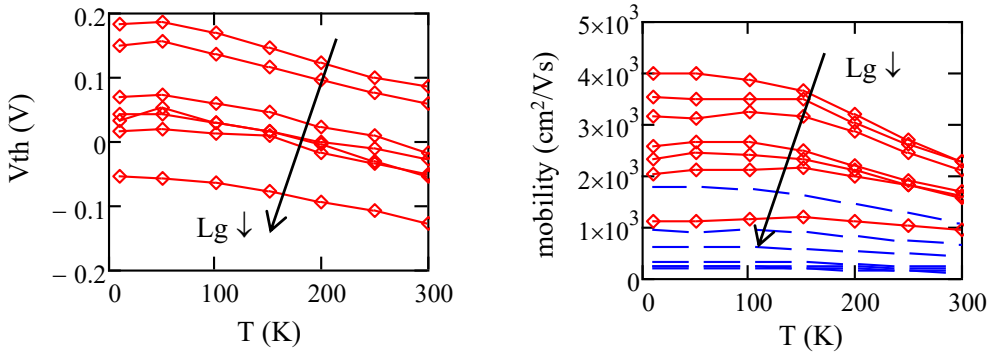


Fig. 3.4. *Variations with temperature of a) threshold voltage V_{th} and b) low field mobility μ_0 (red solid line) and μ_{femax} (blue dashed lines) as obtained on GaN HEMT devices with various gate lengths L_g(nm)= 100, 120, 150, 200, 500, 1000 and 3000 (V_d=50mV, W_g=100µm).*

The variations with temperature of the subthreshold swing $SS=dV_g/dlog(I_d)$ are shown in Fig. 3.5a for various gate lengths. As expected from cryo-operation, the subthreshold swing SS mostly follows the Boltzmann linear trend vs T over 100K before saturating at low temperature, likely due to specific interface trap energy profile and/or charge-induced-disorder potential fluctuations, as found in Si MOS devices [3.24, 3.25].

The access series resistance R_{sd} was extracted using Eq. (3.2) at strong inversion where its impact is maximized. The variations with temperature of the series resistance R_{sd} for various gate lengths are shown in Fig. 3.5b. The access resistance R_{sd} values range typically around 1400 Ω.µm and increases linearly with temperature above 100K, whatever the gate length, emphasizing the R_{sd} extraction consistency. These $R_{sd}(T)$ variations are in line with the metallic degenerate behaviour observed for the sheet resistance of AlGaN/AlN/GaN HEMT structures with $\approx 10^{13}$q/cm^2 2DEG density [3.21, 3.26].

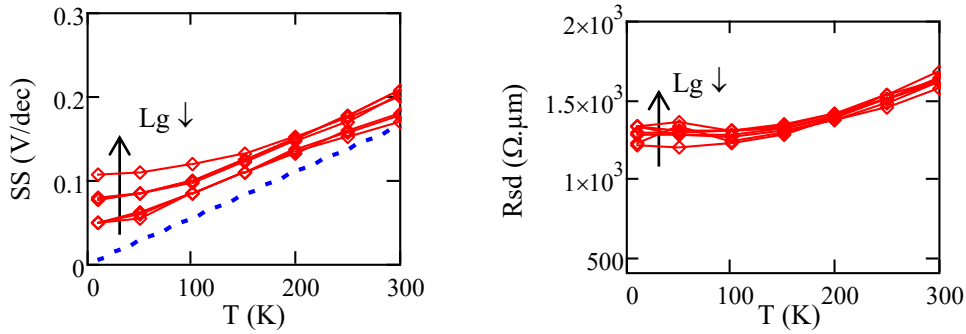


Fig. 3.5. *Typical variations with temperature of subthreshold swing SS (left) and access series resistance R_{sd} (right) as obtained on GaN HEMT devices for various gate lengths L_g (nm)= 100, 120, 150, 200, 500, 1000 and 3000 (V_d=50mV, W_g=100µm).*

3.3.3 Lambert-W-function based MOSFET parameter extraction

Lambert W function-based MOSFET parameter extraction has also been carried oud using Eqs (3.3)-(3.4). Typical fits of the transfer characteristics obtained by LW function modelling over a wide gate voltage range from below to above threshold with optimized parameters (V_{th}, μ_0, n, R_{sd}) are illustrated in Fig. 3.6. Note that excellent fits of the characteristics can be obtained, especially around and above threshold i.e. V_g>-0.25V for $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ curves.

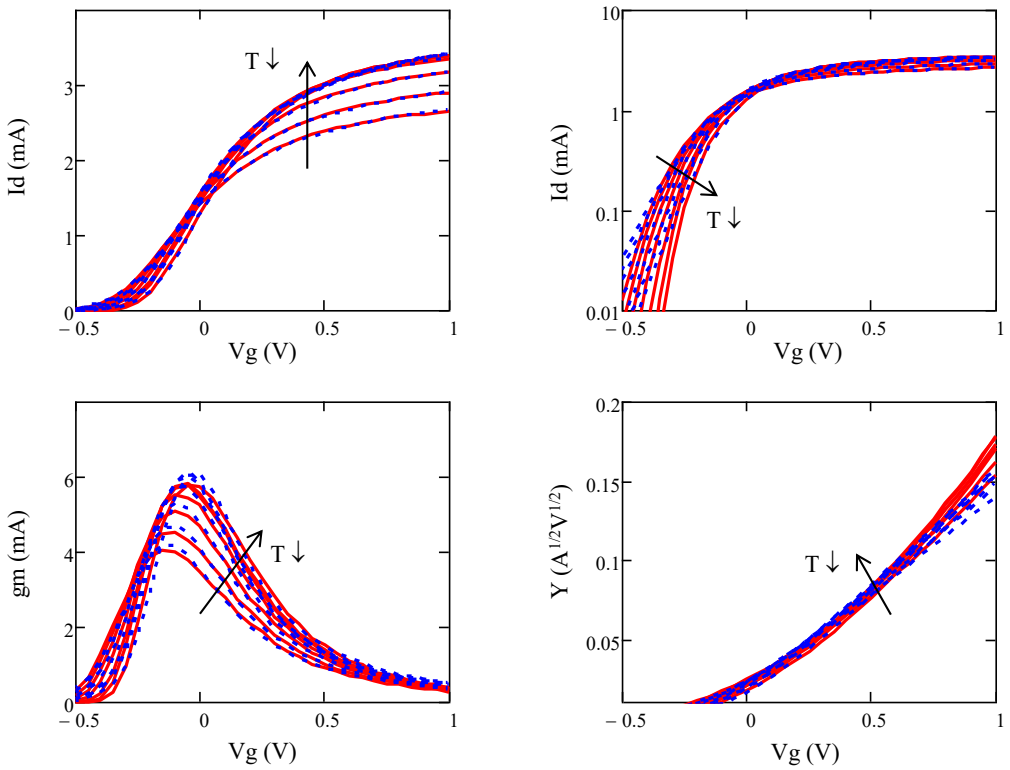


Fig. 3.6. *Experimental (red solid lines) and Lambert-W model fits (blue dashed lines) $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics for various temperatures T(K)= 10, 50, 100, 150, 200, 250 and 300 as obtained on GaN/Si HEMT devices (V_d=50mV, L_g=500nm, W_g=100µm).*

In Fig. 3.7 are shown the variations with temperature of the threshold voltage V_{th} and low field mobility μ_0 obtained with the LW function fitting method (red solid lines) for devices with various gate lengths. For comparison purpose, the V_{th}(T) and μ_0(T) curves extracted with Y-function method (blue dashed lines) are also reminded. Although slightly different, the V_{th} and μ_0 parameters extracted by both methods have the same behaviour with temperature and gate length, which was also observed for Si MOS devices [3.17, 3.18]. The good mobility values obtained by the LW function method confirm the quality of such GaN technology.

In Fig. 3.8 are shown the variations with temperature and reciprocal temperature of the subthreshold ideality factor n_L obtained from the LW function fittings for various gate lengths (red solid lines). The n values directly deduced the subthreshold swing SS (see Fig. 3.5a), n_{SS}=SS/(2.3×kT), are also reported in blue dashed lines. As can be seen, the LW function fitting procedure tends to overestimate the ideality factor, especially at low temperature. However, this inconvenience does not alter the validity of the MOSFET parameter extraction just below and above threshold. It should also be noticed that the 1/T dependence of the ideality factor has been previously found in Si MOSFETs and can be explained by the SS plateauing behaviour at low temperature [3.18].

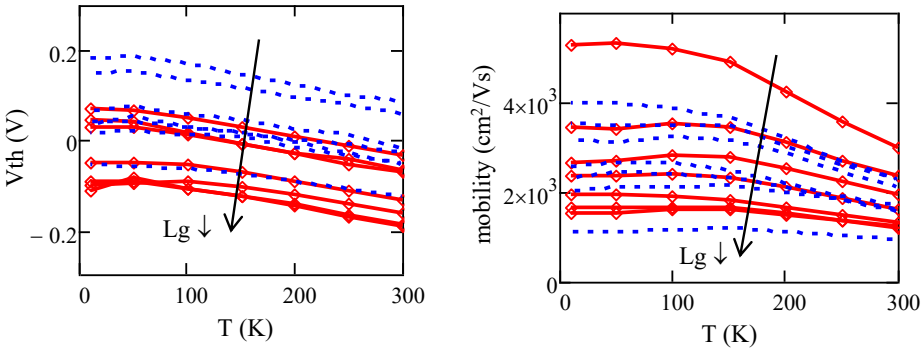
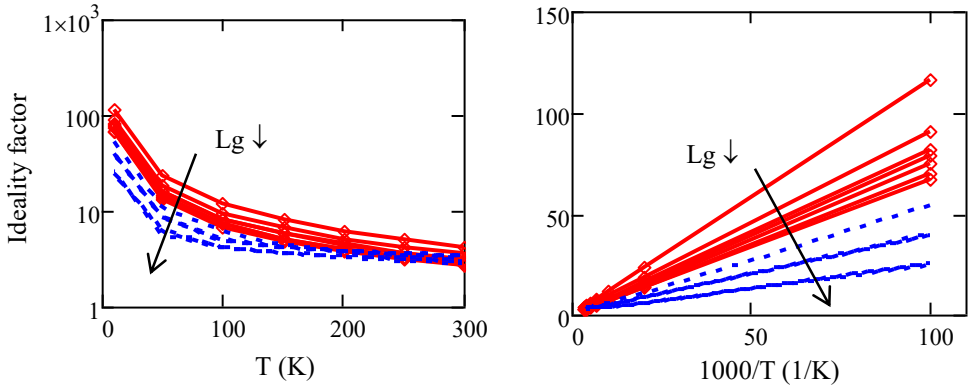


Fig. 3.7. Variations with temperature of a) threshold voltage Vth and b) electron low field mobility µ0, as obtained from LW function extraction (solid line) and from Y-function method extraction (dashed lines) on GaN/Si HEMT devices with various gate lengths Lg(nm)= 100, 120, 150, 200, 500, 1000 and 3000 (Vd=50mV, Lgs=1µm, Lgd=1.5µm, Wg=100µm).

The access series resistance values R_{sd} extracted by the LW function fitting method (red solid lines) are displayed in Fig. 3.9(a) along with those obtained by Y-function method (blue dashed lines) for a transistor with an access region distance $L_{sd}=L_{gs}+L_{gd}=2.5\mu m$, emphasizing the consistency of the two extraction methodologies. In Fig. 3.9(b), are reported the temperature dependence of the source and drain resistance R_{sd} extracted from Y-function method for two access region distances L_{sd1}= 2.5µm and L_{sd2}=11µm for various gate lengths. In this case, a larger temperature dependence of R_{sd} can be noticed for the devices with the longer access region distance.



(a) (b)

Fig. 3.8. *Variations of subthreshold ideality factors n_L (red solid lines) and n_{SS} (blues dashed lines) and b) with temperature (a) and reciprocal temperature (b) as obtained on GaN HEMT devices for various gate lengths L_g(nm)= 100, 120, 150, 200, 500, 1000 and 3000 (V_d=50mV, W_g=100µm).*

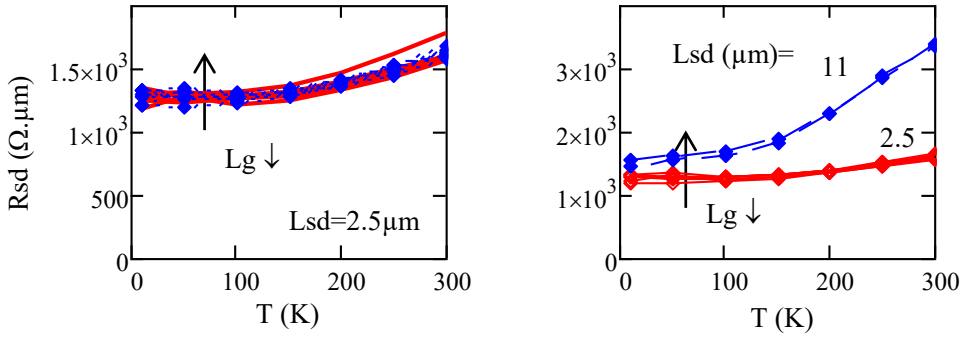


Fig. 3.9. *a) Variations with temperature of series resistance values R_{sd} extracted by LW function method (red solid lines) and by Y-function method (blue dashed lines) as obtained on GaN/Si HEMT devices for various gate lengths L_g(nm)= 100, 120, 150, 200, 500, 1000 and 3000 (V_d=50mV, L_{gs}=1µm, L_{gd}=1.5µm, W_g=100µm). b) Variations with temperature of series resistance values R_{sd} extracted by Y-function method (red solid lines) for two access region distances L_{sd}=2.5µm and 11µm as obtained on GaN/Si HEMT devices for various gate lengths L_g(nm)= 1000 and 5000 (V_d=50mV, L_{gs}=5.5µm, L_{gd}=5.5µm, W_g=125µm).*

In order to discriminate the contribution between the contact resistance R_c and the 2DEG access region resistance $\rho_{2DEG}.L_{sd}$, ρ_{2DEG} being the 2DEG sheet resistance, a TLM analysis of the source-drain series R_{sd} for two L_{sd} values has been carried out using Eq. (3.7),

$$R_{sd}(L_{sd}) = 2.R_c + r_{2DEG}.L_{sd} \quad (\Omega.\mu m). \tag{3.7}$$

By this way, ρ_{2DEG} and R_c can be obtained from,

$$r_{2DEG} = \frac{R_{sd}(L_{sd2}) - R_{sd}(L_{sd1})}{L_{sd2} - L_{sd1}} \tag{3.8a}$$

$$R_c = \frac{R_{sd}(L_{sd1}) - r_{2DEG}.L_{sd1}}{2} = \frac{R_{sd}(L_{sd2}) - r_{2DEG}.L_{sd2}}{2} \quad . \tag{3.8b}$$

In Fig. 3.10(a) are displayed the variations of the contact resistance R_c and the 2DEG sheet resistance ρ_{2DEG} as obtained from Fig. 3.9(b) data using Eqs (3.8) for L_{sd1}=2.5µm and L_{sd2}=11µm. As can be seen, the contact resistance R_c is rather temperature independent (≈550Ω.µm), which reveals a quasi metallic behavior. Instead, the 2DEG sheet resistance ρ_{2DEG} increases significantly with temperature likely due to the mobility increase with temperature lowering, as for long channel mobility in Figs 3.8(b), and a constant polarization-induced 2DEG carrier density. Since, at room temperature, ρ_{2DEG}≈200Ω and μ_0≈2000cm^2/V/s, it follows that the 2DEG electron density in the access regions is about ≈1.5x10^{13}/cm^2, which is for some reason about ≈30% larger than the standard polarization-induced value for the AlGaN/GaN system as measured e.g. by Hall effect in devices from the same technology [3.26, 3.27]. In Fig. 3.10(b) are shown the variation with temperature of the percentage contribution of the 2DEG access region resistance to the total source-drain resistance $R_{sd}=2.R_c+\rho_{2DEG}.L_{sd}$. As can be seen, the contact resistance contribution is enhanced as the temperature is lowered and can reach up to 90% (resp. 70%) for an access region length L_{sd}=2.5µm (resp. 11µm).

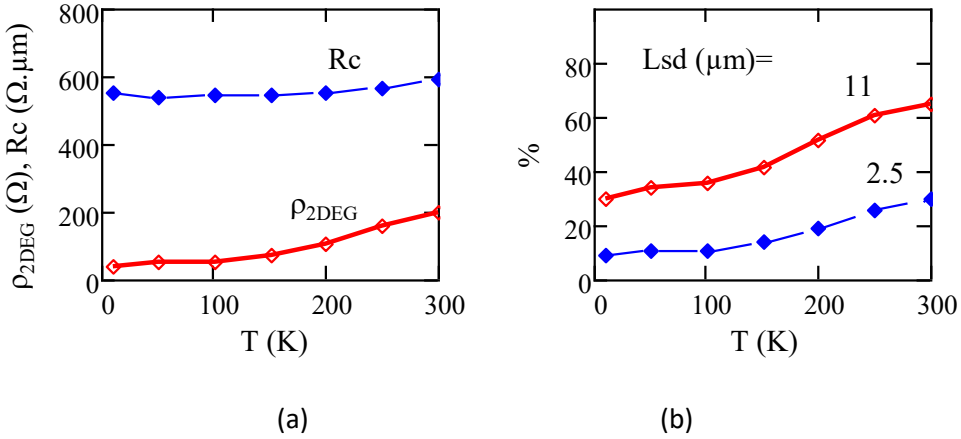


Fig. 3.10. *a) Variations with temperature of the 2DEG sheet resistance ρ_{2DEG} (red solid lines) and of contact reistance R_c (blue dashed lines) as obtained from R_{sd} TLM analysis on GaN/Si HEMT devices with various access region lengths L_{sd}=2.5 and 11 µm. b) Variations with temperature of percentage contribution of 2DEG access region resistance to the total source-drain resistance R_{sd} for two access region distances L_{sd}=2.5µm and L_{sd}=11µm as obtained from Fig. 3.9(b) data.*

Finally, the saturation velocity v_{sat} has been extracted using the Y-function (Eq. (3.5)) and standard (Eq. (3.6)) methods after having recorded the $I_d(V_g)$ characteristics in saturation regime (V_d=5V, not shown here). In Fig. 3.10a are reported the variation with temperature of such extracted saturation velocities for various gate lengths. It should be mentioned that the value of the source resistance R_s needed in Eq. (3.6) was taken, according to Ohm's law, as a portion of the total resistance R_{sd} such as $R_s=L_{gs}/(L_{gs}+L_{gd})$. As can be seen from Fig. 3.10a, the v_{sat} values obtained by the standard method (Eq. (3.6)) are significantly underestimated with respect to those deduced from Y-function, especially when R_s correction is overlooked (R_s=0 in Eq. (3.6)). The overall temperature dependence of v_{sat} is in agreement with those obtained on Si MOS transistors [3.20]. In Fig. 3.10b are shown the corresponding variations of v_{sat} with gate length, revealing as is usual the increase of v_{sat} with channel length reduction, which is inherent to the extraction procedure [3.19, 3.20]. It is worth noting that these saturation velocity values found around 10^7cm/s well agree with those previously reported in GaN HEMTs [3.28-3.32].

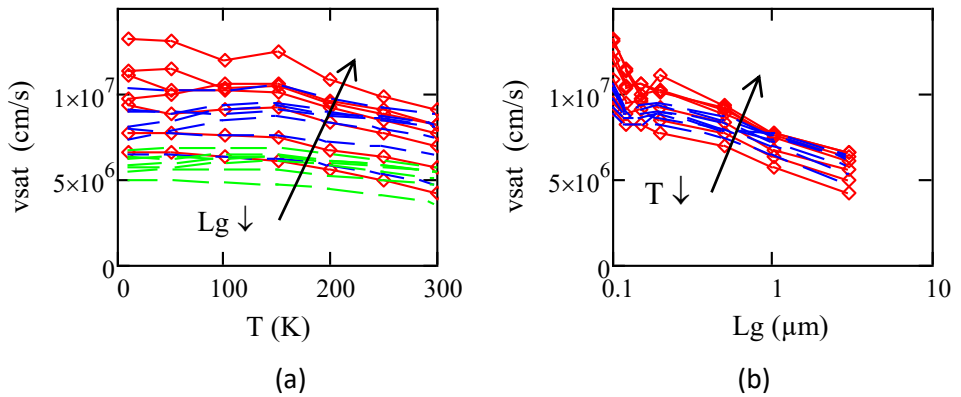


Fig. 3.11. *a) Variations with temperature of saturation velocity v_{sat} as extracted from Y-function (Eq. (3.5)) (red solid lines) and standard method with (blue dashed lines) or without (green dashed lines) R_{sd} correction (Eq. (3.6)) as obtained for various gate lengths L_g(nm)= 100, 120, 150, 200, 500, 1000*

and 3000 (V_g=1.5V, V_d=5V & V_d=50mV, W_g=100µm). b) Variations with gate length of saturation velocity v_{sat} as extracted from Y-function (Eq. (3.5) (red solid lines) and standard method with (blue dashed lines) or without (green dashed lines) R_s correction (Eq. (3.6)) as obtained on GaN/Si HEMT devices for various temperatures.

4 Experimental Assesment of Cryogenic InGaAs HEMTs for Quantum Technologies Down to 10K (contributor: INPG/IBM)

4.1 Introduction

As qubit technologies for quantum computing advance, challenges for the engineering of the entire quantum system become imminent [4.1]. In particular, the study and optimization of low-noise-amplifiers (LNAs) at cryogenic temperature becomes imperative [4.2], as LNAs are needed to amplify the very low-power qubit readout signals. Due to the limited cooling power in the cryostat, and need for thousands of amplified channels, the power dissipation of the LNA technology becomes crucial [4.3]. III-V HEMT technologies like InGaAs/InP offer great interest, as they present extremely high electron mobility, allowing high output at low power consumption [4.4]. Moreover, HEMTs also provide lower noise compared to MOSFETs, by the use of an epitaxial gate barrier rather than oxide [4.5]. To enable a HEMT technology tailored for cryogenic and qubit readout operation, a precise evaluation of their static, noise and thermal performance is needed, along with enhanced understanding of their low-temperature properties. In this work, we have therefore characterized such InGaAs-based HEMT devices in 3 different aspects: DC operation and transport, self-heating effect, and low-frequency noise, from room temperature down to T = 10 K.

4.2 Devices under study

The devices studied in this work are high electron mobility transistors (HEMTs) fabricated by IBM Zurich and consist of an $In_{0.53}Ga_{0.47}As$ channel, stacked in-between two layers of InAlAs, as shown in Fig. 4.1. The InAlAs serves at the bottom as a buffer connecting to a semi-insulating InP substrate, and at the top as a spacer separating the channel from a third layer of InAlAs, to reduce possible gate leakages (Fig.4.1). For the present study, we tested single and double channel devices with channel widths between 10 and 50 µm and channel length spanning from 50 up to 130 nm. In all cases, the distance between source and drain regions was 1.4 µm, except when studying specifically the effect of this parameter.

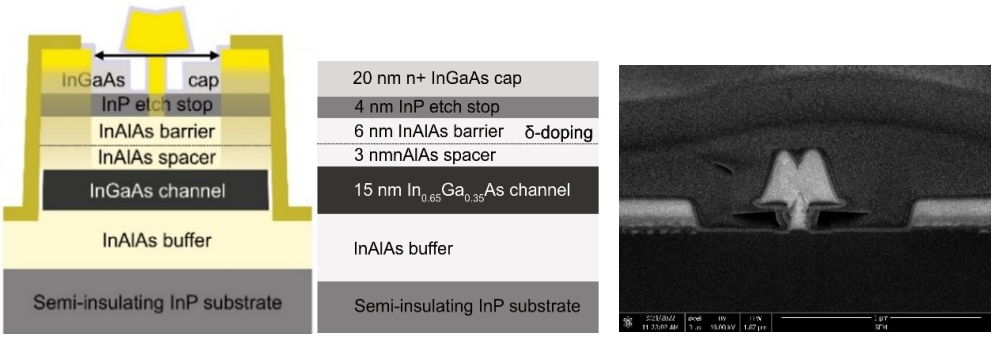


***Fig. 4.1**. HEMT structure under test: schematics (left), layer dimensions (center), TEM of the T-gate structure (right).*

4.3 DC parameters and transport

4.3.1 Initial observations

From the transfer characteristics shown in Fig. 4.2, which are corrected [4.6] with regards to current leakage at high gate voltage, V_g, at a first glance we see how as the temperature decreases, both the threshold voltage, V_t, and the mobility increase. Moreover, a knee in the curve can be observed above V_g = 0.1 V for low temperatures, which we attribute to the onset of the population of the L valley [4.7, 4.8] addressed in detail in a following section. This effect becomes even more evident when plotting the transconductance, $g_m=dI_d/dV_g$ (Fig. 4.3), where, beside the peak value boost going towards 10K, a clear second peak appears in strong inversion, corresponding to the L valley conduction. Concerning the subthreshold slope, Fig. 4.4 clearly shows that it consistently increases as temperature decreases, whereas we see both a degradation of the slope and a roll-off of V_t due to short channel effect (SCE) [4.9] for the shortest channel regardless of T.

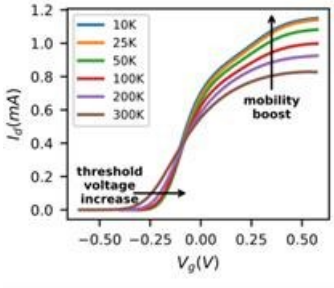


Fig. 4.2. *Transfer characteristics for W = 10µm and L_g = 70 nm (V_d=30mV) at various temperatures.*

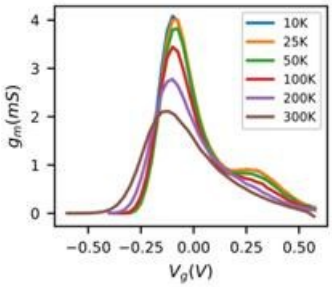


Fig. 4.3. *Transconductance characteristics for W = 10µm and L_g = 70 nm (V_d=30mV) at various temperatures.*

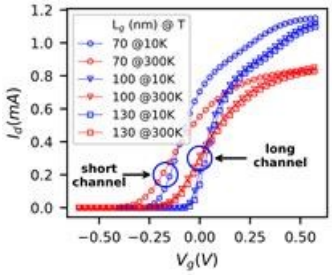


Fig. 4.4. *Transfer characteristics for different channel lengths at T = 10 and 300K.*

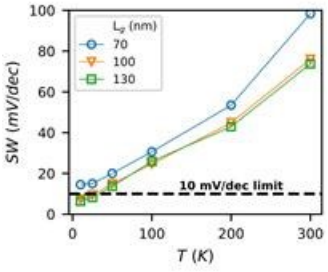


Fig. 4.5. *Extracted values of subthreshold swing versus T for various gate lengths.*

4.3.2 Extraction of DC parameters

As can be seen from Fig. 4.5, the extracted subthreshold swing (SW) at room temperature is much lower with respect to the values measured in InGaAs-channel MOSFETs [4.8], highlighting the improvement achieved by the elimination of the Al oxide interface traps. In addition, we note that as T decreases below 25K for the longer channels, SW reaches values close to 6mV/dec. This value is significantly lower than 10 mV/dec, which is the reported lower limit for both Si [4.10] and InGaAs MOSFETs [4.8], attributed to disorder-induced band tails [4.11]. We claim that the high quality of the 2DEG/buffer interface helps overcoming this SW limit and achieving lower operating voltages.

Extraction of low-field mobility, μ_0, and threshold voltage, V_t, has been performed using the series resistance-immune Y-function (4.1) [4.12],

$$Y = I_d/\sqrt{g_m},\ \ Y' = Y\sqrt{1-\theta_2\left(V_g - V_t\right)^2} \tag{4.1}$$

after a corrective iteration to account for the mobility attenuation factor θ_2 [4.13]. The linearity of $Y(V_g)$ is affected at low temperatures (LT) by the onset of the L valley (Fig. 4.6), confirming results in III-V MOSFETs [4.8]. We nonetheless verified that taking into account an average slope of Y (Fig. 4.7(c)) within a range of V_g representing strong inversion, yet before eventual leakages, we can extract the combination of average $\mu_{0,avg}$ and V_t that best fit the original trans-characteristics (Fig. 4.7(a)) using (4.2).

$$I_d = \frac{WC_{ox}V_d(V_g - V_t)}{L}\frac{\mu_{0,avg}}{1+\theta_1(V_g-V_t)+\theta_2(V_g-V_t)^2} \tag{4.2}$$

Following a different approach, Fig. 4.7(d) shows that if the linear fit of $Y(V_g)$ is done only on its strictly linear part, which is the V_g range corresponding to Γ valley conduction, it allows the isolated extraction of the Γ valley mobility, $\mu_{0,\Gamma}$ (Fig. 4.8), which is far higher than results from [4.8, 4.10]: the 2DEG proves to preserve the high value of III-V mobility. Moreover, when looking at both $\mu_{0,\Gamma}$ and $\mu_{0,avg}$ (Fig. 4.9), we see how phonon scattering reduction at lower T causes an increase of mobility. Furthermore, μ_0 is consistently lower as the gate channel shortens likely due to stronger effect of neutral impurity scattering, as also observed in III-V MOSFET [4.8] and Si MOSFETs [4.14].

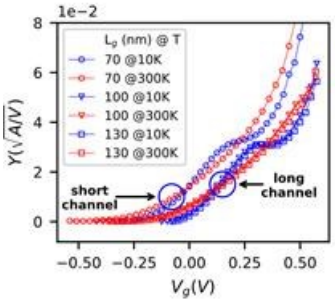


Fig. 4.6. *Y-function versus gate voltage for different channel lengths at T = 10 and 300K.*

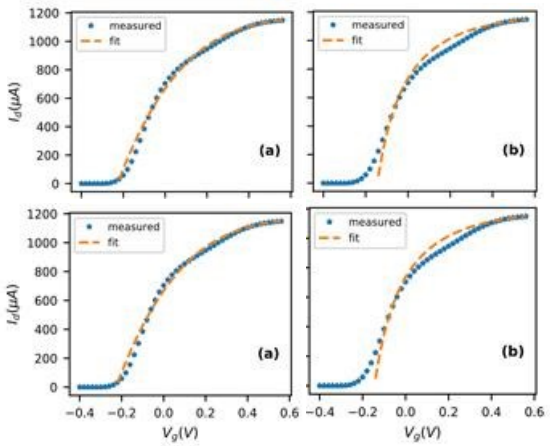


Fig. 4.7. *Y-function linear fit over a broad V_g span (b) and a narrow one (d) and respective $I_d(V_g)$ (a and c) reconstruction through (2).*

An additional indication of L valley conduction is found when comparing $\mu_{0,\Gamma}$ and $\mu_{0,av}$: as L conduction is much more affected by phonon scattering due to higher effective mass, the average mobility drops to lower values. This is also evident by the lower value of the 2nd peak of g_m at low T (Fig. 4.3). Finally, Fig. 4.10 shows that the extracted V_t value increases as T lowers from 300 K down to 100 K, following the Boltzmann statistics, yet it saturates at very low temperatures due to the onset of degenerate behavior [4.15]. Also, it is easy to confirm the SCE, as all the L_g = 70 nm values are significantly lower.

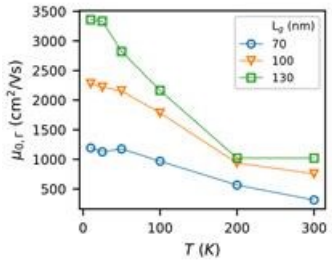


Fig. 4.8. *Extracted Γ valley low-field mobility from Y-function linear fit in the Γ interval (Fig. 7d) versus T for different gate lengths.*

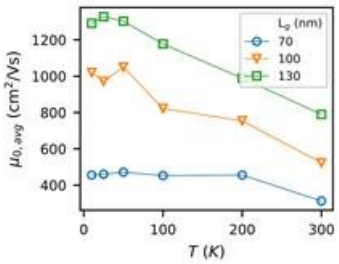


Fig. 4.9. *Extracted average low-field mobility versus T for different gate lengths.*

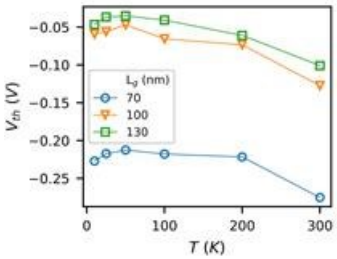


Fig. 4.10*. Extracted threshold voltage with Y-function versus T for different gate lengths.*

4.3.3 Impact of access region length

From Fig. 4.11, we can observe how various distances in between the source and drain regions, L_{SD}, influence differently the current degradation at high V_g. This difference is much stronger at higher temperature, while becoming almost negligible at 10K. We can also clearly see that, as expected thanks to the suppression of SD series resistance, R_{sd}, the corresponding Y-function (Fig. 4.12) is not affected by L_{SD}: the curves merge at each temperature, as W_g and L_g are identical for all three devices. The R_{sd} was extracted through (4.3)

$$\theta_1 = \theta_{1,0} + \frac{WC_{ox}V_d\mu_{0,avg}}{L}R_{sd} \tag{4.3}$$

around 380 Ω regardless of T and L_{SD}, indicating that it is dominated by the SD contact resistance.

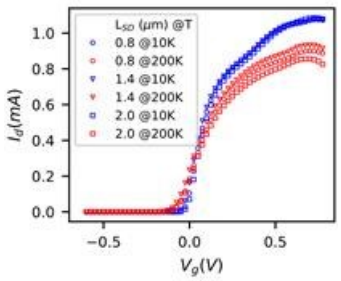


Fig. 4.11. *Transfer characteristics for W = 10μm, L_g = 100 nm and different Source-Drain distances at 10 and 200K (V_d = 30 mV).*

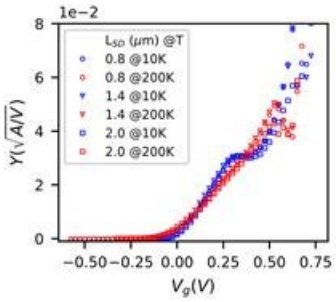


Fig. 4.12. *Y-function characteristics for W = 10μm, L_g = 100 nm and different Source-Drain distances at 10 and 200K (V_d = 30 mV).*

4.4 Self-Heating Effect

On devices with fixed W_g = 10 μm and L_g spanning from 200 down to 50 nm, we performed gate resistance thermometry measurements by recording the current flowing in between two metallic pads connected to the gate (Fig. 4.13) and biased with a small differential voltage ΔV_g of 30 mV. As the drain voltage, V_d, increases and we move towards saturation region, the current flowing in between the gate pads decreases due to an increase in resistance, caused by the self-heating of the device (Fig. 4.14). As we extract the gate resistance ($R_g = \Delta V_g/\Delta I_g$) in between the pads at the beginning (V_d=0) and end of each measurement (Fig. 4.15), we can compute the temperature variation ΔT from (4.4),

$$\Delta T = \frac{R_{g,final} - R_{g,initial}}{s} \quad (4.4)$$

where s is the slope of $R_g(T)$ after interpolation. This way we account for the self-heating at every ambient temperature (Fig. 4.16) and versus the dissipated power ($P=I_d.V_d$) in the channel (Fig.4.17). In Fig. 4.16 we observe how longer channels consistently heat up more with respect to a shorter one: as the mean free path is around 200 nm in these devices, the influence of scattering-induce self-heating should increase with L_g. Also, the linear increase of ΔT with the power in Fig. 4.16 can provide the thermal resistance $R_{th} = \Delta T/P$ [4.16]. Finally, Fig. 4.18 demonstrates that the HEMTs under study, being bulk-like devices, have a very good heat dissipation like state-of-the-art bulk Si CMOS [4.17] and close to III-V HEMT results [4.18], yet preserving this value at 10 K and exhausting heat overall much better than FDSOI Si MOSFETs [4.16].

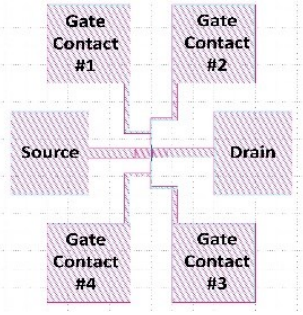


Fig. 4.13. *Contact pad schematics of dedicated structures for gate thermometry.*

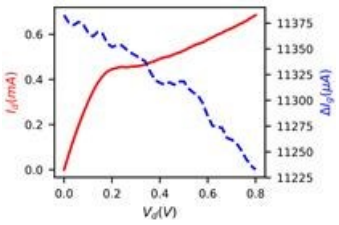


Fig. 4.14. *Raw measurement of gate resistance thermometry for W = 10 μm and L_g = 100 nm at T = 10K.*

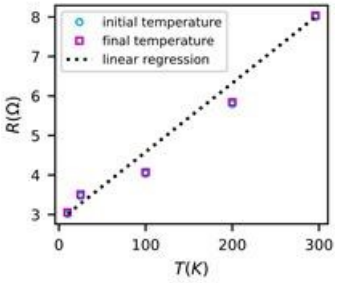


Fig. 4.15. *Resistance of the gate metal vs temperature at initial and final stages of measurement.*

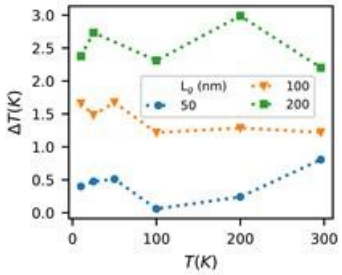


Fig. 4.16. *Extracted temperature variation (Self Heating) for W = 10μm and different channel lengths versus temperature.*

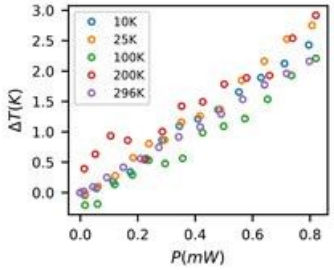


Fig. 4.17. *Self Heating for W = 10μm and L_g = 200nm versus dissipated power in the channel.*

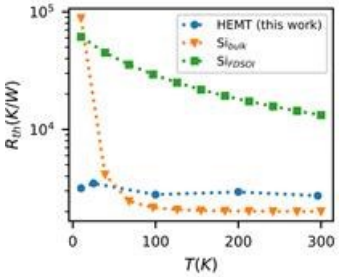


Fig. 4.18. *Thermal resistance versus temperature for different technologies.*

4.5 Low-frequency Noise

In heterostructure HEMTs, the lack of oxide may affect the uniformity of traps at the channel interface, especially when considering small devices. Figs 4.19 and 4.20 show however that for the measured 2-channel device with W_g = 50 um and L_g = 130 nm, the overall drain current power spectra at both 300 and 10 K abide a 1/f-like behavior, indicating a uniform distribution of traps. The extracted noise spectral density at 10 Hz (Fig. 4.21) seems to follow a ~$1/I_d$ trend in the low drain current range, revealing a dominance of channel mobility fluctuations (Δμ), expressed by (4.5) [4.19],

$$\frac{S_{id}}{I_d^2} = q\mu_0 C_{ox} V_d \frac{\alpha_H}{fL^2 I_d} \quad , \quad (4.5)$$

where α_H is the Hooge parameter. This effect usually takes place in bulk-conducting devices, such as the HEMTs in this work, which indeed conduct mainly in the volume of InGaAs before reaching strong inversion at the surface with InAlAs. Above V_t, the data is well fitted with the Carrier Number Fluctuation (Δn) model (4.6) [4.20],

$$\frac{S_{id}}{I_d^2} = S_{Vfb}\left(\frac{g_m}{I_d}\right)^2, S_{Vfb} = \frac{q^2 kTN_{st}}{WLC_{ox}^2 f^\gamma}\ , \tag{4.6}$$

meaning that the trapping/detrapping of carriers in the InGaAs/InAlAs interface traps takes the lead once the channel is formed. These two noise mechanisms were both found to be still active at 10 K (Fig. 4.22). The extracted interface trap density, N_{st}, shown in Fig. 4.23, was found to be significantly lower than the AlO_3-based InGaAs MOSFETs studied in [4.8] and measured here for comparison, confirming the interface superiority of HEMTs. Furthermore, when compared to industry-level FDSOI MOSFETs [4.21], the N_{st} of HEMTs is found to be higher at 300 K, while outperforming them for T < 100 K. As a result, the HEMT area-normalized flat-band voltage noise, S_{vfb} (4.6), which is a direct measure of the equivalent gate voltage noise, is significantly lower than FDSOI MOSFETs from 50 K and below (Fig. 4.24), revealing a promising advantage for amplifier applications, where the input signal-to-noise ratio is critical.

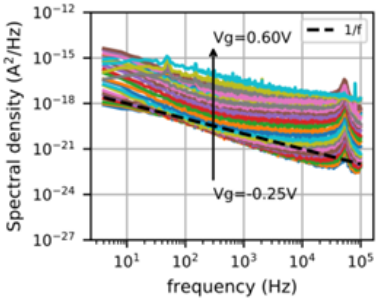


Fig. 4.19. *Measured drain current noise spectra for W =50 µm and L_g = 130 nm at T = 300K.*

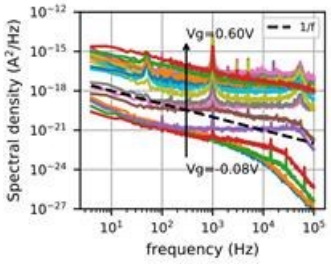


Fig. 4.20. *Measured drain current noise spectra for W =50 µm and L_g = 130 nm at T = 10K.*

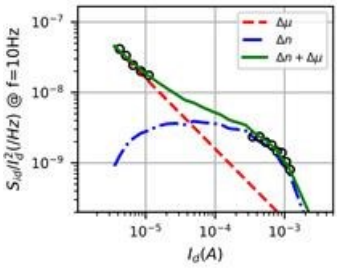


Fig. 4.21. *Normalized drain current noise at f = 10 Hz with Δn (6) and Δµ (5) fittings at 300K (W = 50 µm and L_g = 100 nm, V_d = 30 mV).*

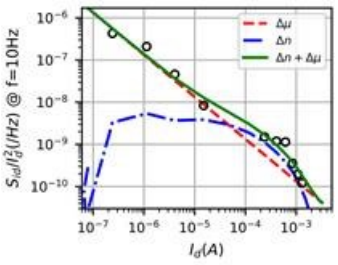


Fig. 4.22. *Normalized drain current noise at f = 10 Hz with Δn (6) and Δµ (5) fittings at 10K (W = 50 µm and Lg = 100 nm, Vd = 30 mV).*

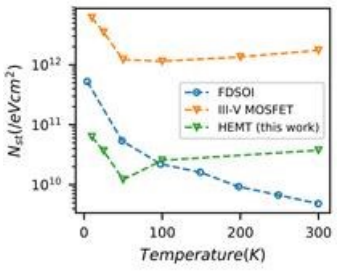


Fig. 4.23. *Extracted interfacial trap density versus temperature for different technologies.*

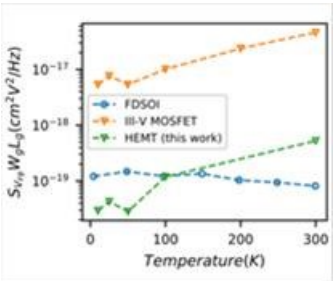


Fig. 4.24. *Extracted flat-band voltage power spectral density S_{Vfb} at f = 10 Hz versus temperature for different technologies.*

5 Cryogenic spectroscopy of border traps by C-G-V-f measurements and TCAD simulations in III-V devices (contributors: Tyndall)

5.1 Introduction

The results presented and discussed here are the continuation of the work presented in section 1.3 of D2.3. The border traps analysis in the Al_2O_3/InGaAs system is expanded to other MOS structures with different high-k dielectric (HfO_2 in addition to Al_2O_3) and the corresponding p-type samples are also discussed. The methodology for border traps spectroscopy which rely on physics-based simulation of metal-oxide-semiconductor (MOS) systems is demonstrated in this section on the Al_2O_3/n-InGaAs system at low temperature (-50°C) using the Ginestra® software package.

5.2 High-k/p-InGaAs MOS impedance at cryogenic temperature

Figure 5.1 shows the C-V data measured at room temperature and at 10K for Au/Ni/Al_2O_3/p-InGaAs/InP and Au/Ni/HfO_2/p-InGaAs/InP MOScaps. The Al_2O_3 sample is the twin sample to the n-type InGaAs MOScap described in D2.3. Both Al_2O_3 MOS capacitors received identical surface treatment, ALD dielectric and post deposition thermal treatment. The full experimental details are described in D2.3.

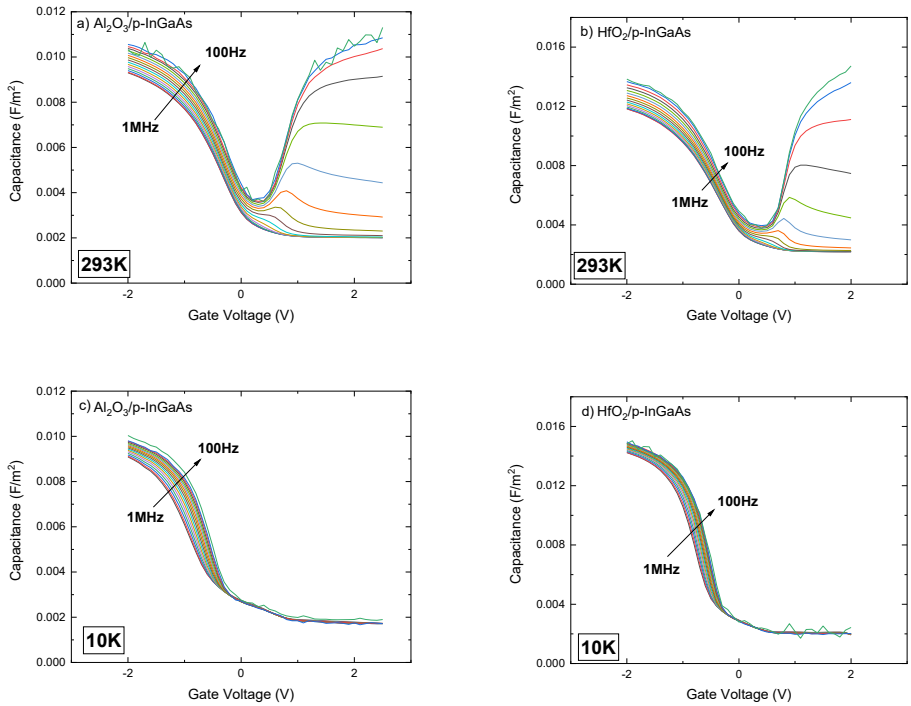


***Fig. 5.1**. Multi-frequency C-V characteristics measured at room temperature a) and b) and at 10K c) and d) on an Au/Ni/Al_2O_3/p-InGaAs/InP and Au/Ni/HfO_2/p-InGaAs/InP MOScaps.*

Similar to the n-type MOScap results shown in D2.3, at 10K the frequency dispersion reduces across the full voltage range from depletion to accumulation (Fig. 5.1 c) and d)). The minority carrier response in inversion is a thermal process and is fully suppressed at 10K. In accumulation, the fre-

quency dispersion is caused by free majority carriers communicating with traps in the oxide. We have shown previously (D2.3) that the inelastic band-to-trap tuneling model involving a non-radiative multi-phonon process describes accurately the measured characteristics at room temperature. However, unlike the n-type MOS sample the frequency dispersion in accumulation only drops from ~3% (per decade frequency) at 293K to 2% at 10K for the Al_2O_3/p-type MOScap (as compared to the n-type sample 2% down to 0.4%). Previously published studies focused on n-type InGaAs [5.1], [5.2]. The p-type InGaAs MOS devices enable us to explore oxide trap distributions with energy levels aligned or close to the InGaAs valence band. The data of Fig. 5.1 show that significant hole capture and emission by oxide border traps is still taking place at 10K. At such low temperature, phonon assisted capture and emission mechanisms are expected to be suppressed. The observed capacitance dispersion demonstrates that hole capture and emission from the InGaAs valence band to the oxide traps present an important tunnelling component.

At low temperature, it must be noted that the capacitance value in absolute terms decreases for both n (7.5%) and p (3%) Al_2O_3/InGaAs MOS capacitors (D2.3 figure 2.8 a) and c) and Fig. 5.1 a) and c) respectively). The dielectric constant of Al_2O_3 was reported to strongly decrease with temperature [5.3] and this factor could explain the observed trend in the Al_2O_3 devices.

It is interesting to note the analogous behaviour of the HfO_2 and Al_2O_3 MOS devices. The HfO_2/n-InGaAs MOScap also shows the suppression of the dispersion in capacitance across the whole voltage range at 10K (data not shown) while its corresponding p-type device still exhibit hole trapping and emission at 10K (Fig. 5.1d)). This result indicates that these two different dielectrics present defect bands with energy distributions similarly aligned to InGaAs energy band structure.

In contrast with the Al_2O_3/p-InGaAs MOScaps, the HfO_2/p-InGaAs devices show an increase of capacitance (in absolute terms 0.012F/m^2 to 0.014F/m^2 at 1MHz) in accumulation. This behaviour, which wasn't observed on the HfO_2/n-InGaAs devices, is concomitant with a steeper transition from depletion into accumulation of the p-InGaAs interface. This result shows that the p-InGaAs surface may not be in fully accumulated at room temperature and more significantly the defects responsible of the Fermi level pinning present an energy barrier which prevent hole capture at 10K temperature resulting in steeper CV characteristics. This interpretation is also confirmed by CV hysteresis data (not shown) obtained on the HfO_2/p-InGaAs MOScaps where the hysteresis window becomes narrower at 10K due to the reduced hole trapping at 10K. This result confirms that oxide defects are the dominant hole trapping centres over interface states in the high-k/InGaAs system. This result also has potential implications on the operation of InGaAs p-FETs comprising HfO_2 as a gate dielectric at 10K and below.

5.3 Frequency dispersion in accumulation capacitance

In this part, we will discuss the dependence of the accumulation capacitance with frequency at various temperatures for all four devices investigated in this study. Figure 5.2 summarises the measured accumulation capacitance for all four samples at room temperature, -50°C and 10K.

A linear dependence on log(f) of the capacitance is observed at room temperature and -50°C. This behaviour was reported as a characteristic of free carriers capture and emission by bulk-oxide traps through a pure tunnelling mechanism for which the time constant is an exponential function of thickness [5.2]. However, this interpretation fails to explain the strong dependence of the frequency dispersion with temperature as discussed also in section 5.2.

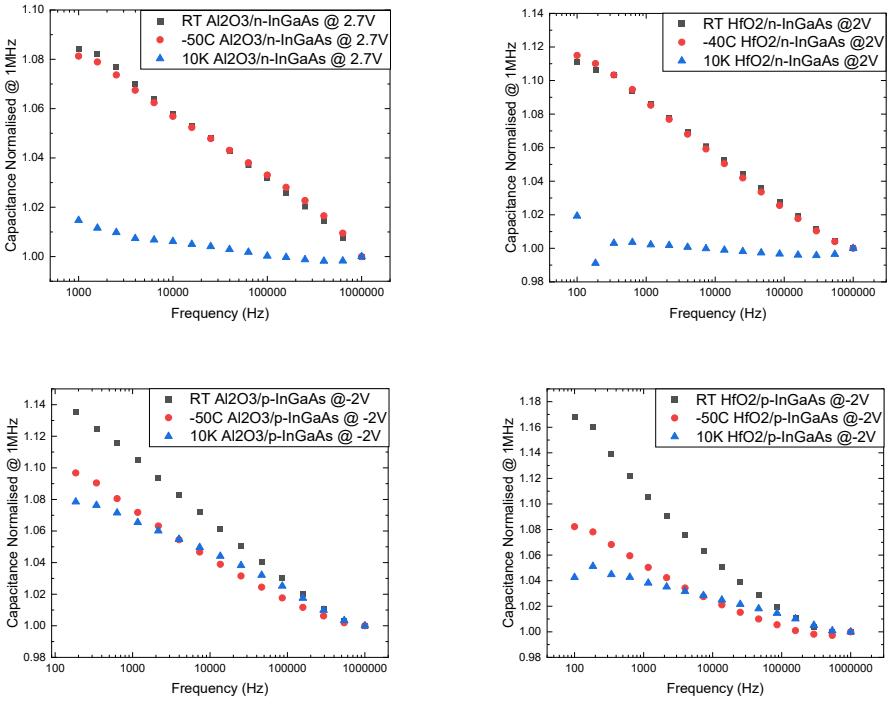


Fig. 5.2. *Accumulation capacitance measured at room temperature, -50°C and 10K for Al_2O_3/InGaAs (n&p) MOScaps a) and c) and for HfO_2/InGaAs (n&p) MOScaps b) and d). The capacitance values were normalised by the 1MHz capacitance value.*

5.4 C-V and G-V Ginestra® simulations

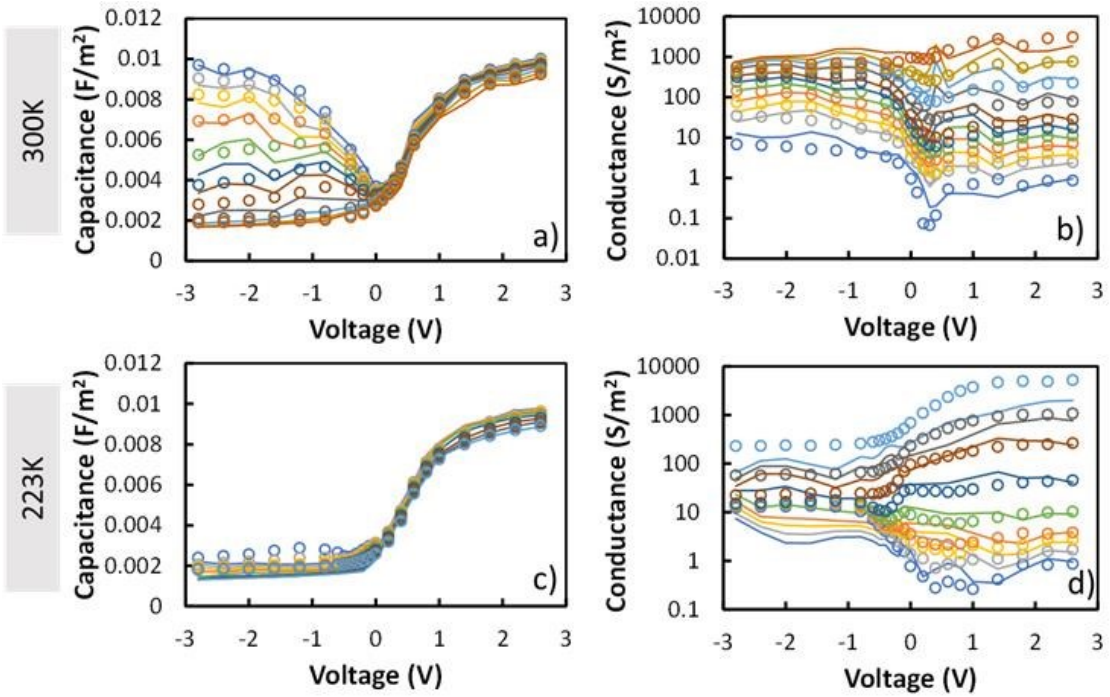


Fig. 5.3. *Multi-frequency C-V (a) and c)) and G-V (b) and d)) data measured (colour circles) and simulated (line) at room temperature and -50°C for Al_2O_3/n-InGaAs structures. Frequency range 1kHz-1MHz.*

The Ginestra® software package is a multi-physics, multi-scale material/device simulation platform which enables the link between material properties (either calculated using DFT or extracted from electrical measurements) and device electrical performances. Ginestra allows exploring the material/defect effects on the device electrical performance.

Figure 5.3 shows the C-V and G-V data measured on the Au/Ni/Al_2O_3/n-InGaAs/InP MOScaps at room temperature and -50°C. The simulated C-V and G-V data at both temperature show excellent agreement with the experimental data. The extracted trap distribution (in energy and space), mapped in Fig. 5.4, shows a significant amount of interface traps (mainly affecting the capacitance) and near-interface/bulk traps (mainly affecting the conductance). More effort is ongoing to collect more experimental C-V and G-V data and use simulations to match C-V and G-V characteristics at different temperatures in order to understand defect influence at cryogenic temperature.

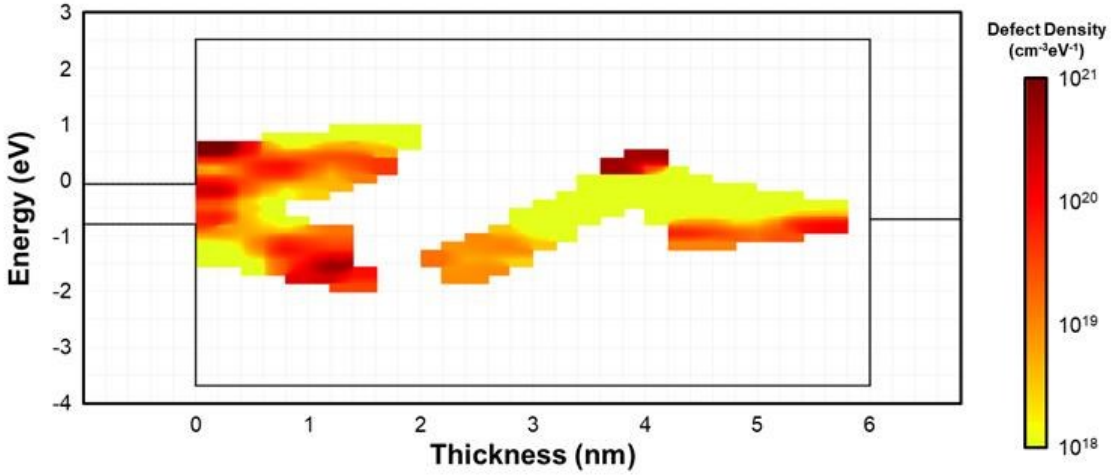


Fig. 5.4. *Extracted energy and space trap distribution that produced the best agreement between the experimental and simulated C-V and G-V data.*

6 RF characterization of III-V HEMTs operated at cryogenic condition (contributor: IAF/FhG)

A highly scalable small-signal and noise model for high-electron-mobility transistors (HEMTs) has been developed throughout the project. The model has been described in detail in previous deliverables and is published [6.1]. Both single HEMT devices as well as low-noise amplifier (LNA) circuits have been used to verify the model. Furthermore, the model has already been used for cryogenic monolithic microwave integrated circuit (MMIC) design in Workpackage 3. The resulting circuit results, which show an excellent agreement with the measurements, serve as an additional proof that the model parameters have been extracted correctly and that the model is capable of being used in high performance cryogenic circuit design.

The model is now used to get a better insight into the noise properties of Fraunhofer IAFs 50 nm metamorphic HEMT (mHEMT) technology especially at cryogenic operation. The most relevant model parts are briefly recapped in the following. More detailed information is provided in the previous deliverables of SEQUENCE and [6.1]. Fig. 6.1 shows the intrinsic model including the most dominant sources of noise.

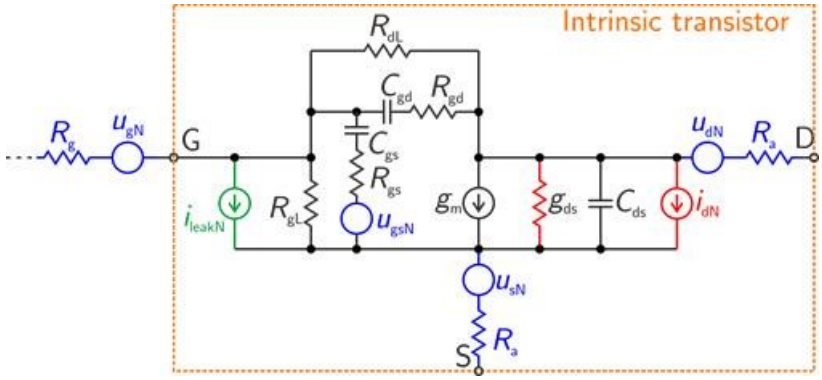


Fig. 6.1. Intrinsic equivalent circuit model core including noise sources. Thermal noise sources of passives are depicted in blue, shot noise caused by gate-leakage current is marked in green, and the channel noise is drawn in red.

The intrinsic noise model is an adaption of Pospieszalski's approach [6.2] and adds a source of pure shot noise to the input of the intrinsic model. This shot noise is caused by gate-leakage flowing through the Schottky gate barrier that needs to be thinned for proper channel control at 50 nm gate length. The shot noise is fully determined by the DC current flowing in the gate.

Pospieszalski's model contains two sources of noise that are only weakly correlated: One related to the input, which is of thermal origin related to R_{gs}, and one related to the output of the intrinsic core related to the output conductance g_{ds}. The later one is generally modelled as thermal noise although it is not necessarily of thermal origin. It is modelled at a temperature T_d exceeding the temperature of the lattice significantly.

T_d is bias dependent, which has been reported by several groups [6.2, 6.3, 6.4]. The high values of T_d have been motivated to be caused by the high electrical field placed across the short gate in on-state bias putting electrons to higher energy levels, which can be interpreted as a higher temperature of the two-dimensional electron gas (2DEG).

This scalable small-signal and noise model can now be used to optimize the cryogenic performance of HEMT LNAs dedicated to quantum bit (qubit) read-out. Todays most promising implemen-

tation of quantum bits are Transmons, which already demonstrated systems with more than 100 qubits [6.5].

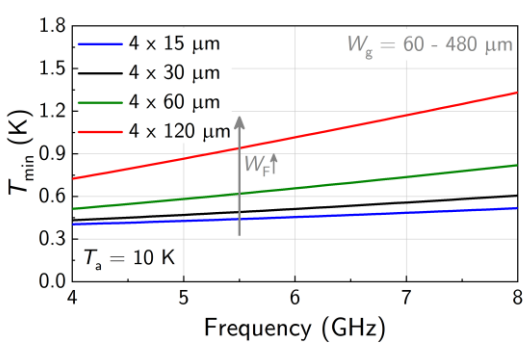
The read-out is currently done using hybrid assemblies, which offer the best noise performance [6.6] to date, but tend to be too bulky to further scale such quantum computers [6.7]. Monolithic integration would reduce the footprint of the amplifiers drastically and allow for multi-channel or multifunctional chips, which would allow for further scaling of the read-out electronics. However, the noise performance of MMICs does not reach the performance of the hybrids in C-band yet. This is due to the fact that on-chip matching networks have more losses compared to matching networks on dedicated low-loss substrates, where the line width of a 50 Ohm line can be chosen one order of magnitude higher compared to on-chip structures. Therefore, improving the noise performance of the active devices is a key to achieve best noise performance with monolithic integrated circuits. Besides of transistor technology improvement (see deliverable 2.3 and [6.8]), this task can only be done with extensive modelling to allow for the fine-tuning of LNA circuits.

The qubit state of Transmons is in most applications measured in C-band (4 – 8 GHz) using traveling wave parametric amplifiers followed by HEMT LNAs. Therefore, an analysis (based on the new scalable small-signal and noise model) how the noise performance of HEMT LNA MMICs can be further improved is given in the following.

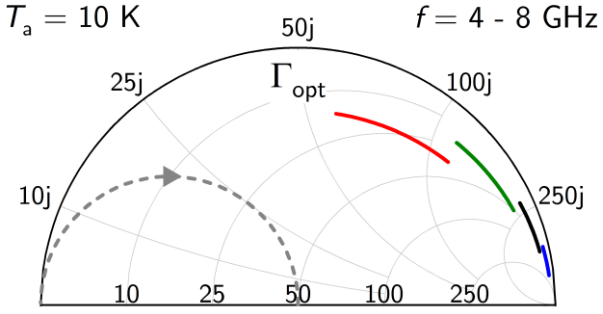
The noise performance of any (active) device is specified by its three (or four real valued) noise parameters, namely the minimum noise temperature T_{min}, the optimal source reflection coefficient Γ_{opt} and the equivalent noise resistance R_n. The noise parameters describe a paraboloid over the Smith chart of the source reflection coefficients. This canonical representation of a noisy two-port can be calculated from its noiseless equivalent circuit with the corresponding noise sources attached [6.9, 6.10] (see Fig. 6.1).

T_{min} specifies the minimum effective input noise temperature T_e that can be reached (heights of the minimum of the paraboloid), when the optimal source reflection coefficient Γ_{opt} (position of the minimum in the Smith chart) is seen by the device. R_n is a measure of how sensitive the device is to mismatch from the optimal source reflection coefficient. It is specifying the steepness of the noise paraboloid over the Smith-chart. Therefore, a higher R_n means that the noise performance is degrading at a higher rate when the device is mismatched from Γ_{opt}.

The task during LNA design is to simultaneously match the input of the device (especially of the first amplifier stage due to Friis equation [6.11]) for power and noise. This can be visualized by transforming the HEMT S_{11} and Γ_{opt} to the centre of the Smith-chart. Based on the cryogenic model, the noise parameters of HEMTs with different gate geometries is investigated. **Fig. 6.2** shows the noise parameters of common-source mHEMTs with 50 nm gate length when the unit gate width (single finger width) W_F is varied at 10 K. Additionally, the maximum stable gain is shown.



(a)



(b)

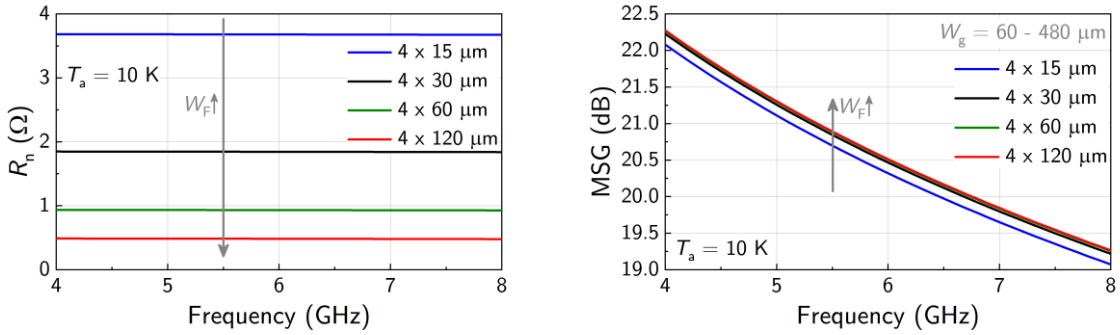


Fig. 6.2. Modelled noise parameters and gain of four finger mHEMT devices with 50 nm gate length and different unit gate width operated at 10 K when biased at V_d = 0.3 V and I_d = 50 mA/mm. The (a) minimum noise temperature T_{min}, (b) optimal source reflection coefficient Γ_{opt}, (c) equivalent noise resistance R_n, and (d) maximum stable gain (MSG) are shown. Devices with an absolute gate width of W_g = 4 × 15 µm (blue), W_g = 4 × 30 µm (black), W_g = 4 × 60 µm (green), and W_g = 4 × 120 µm (red) are depicted.

The minimum noise temperature T_{min} increases with increasing unit gate width. It is likely that the main driver of this is the increasing absolute gate line resistance. As expected, T_{min} increases with frequency since the device gain decreases and output related noise is suppressed at a lower amount. At first glance, devices with low unit gate width seem to be the candidates of choice for best noise performance. However, one needs to take into account the other noise parameters as well.

R_n decreases with increasing unit gate width, which eases broadband noise matching since larger devices are less sensitive to noise mismatch (Fig. 6.2 (c)).

In C-band, Γ_{opt} turns very close to the open-circuit impedances in the Smith-chart for low absolute gate width devices. When the gate width is increased Γ_{opt} turns closer to lower impedances (see Fig. 6.2 (b)) due to the higher input capacitance. For higher unit gate width Γ_{opt} also turns closer to the centre of the Smith-diagram since the higher gate resistance introduces higher losses. To noise-match a HEMT one needs to transform Γ_{opt} to 50 Ohms (Smith-chart centre) by applying an appropriate input matching network. Such a network will in reality always add losses to the input of the active device and consequently, degrade its T_{min}. This is especially true for on-chip matching networks, which cannot be designed as low loss as on dedicated substrates. In general, the implementation of a larger impedance transformation introduces more losses and more bulky networks are needed. Therefore, one would target to achieve this matching with the most lean / low-loss network possible.

An elegant way to perform noise matching with as few components as possible is to use a single shunt inductor at the device input. An ideal lossless shunt inductor will transform Γ_{opt} on a circle of the admittance smith-chart, as depicted in Fig. 6.2 (b). A real inductor will have some losses which slightly changes the transformation. However, the lossless analysis is a sufficiently precise approximation for the transformation of low loss inductors. Fine tuning is performed by accurate CAD models in the end. The simplest network could be achieved by using a device, which is big enough that its Γ_{opt} lies directly on the 50 Ohm admittance circle so that it can be transformed just using the shunt inductor.

However, such a device would need a very large gate width as it can be seen from Fig. 6.2 (b). This has several drawbacks. A larger absolute gate width translates to higher T_{min}, which might

worsen the noise performance. A reason is the high absolute resistance of the gate line for very long fingers. A way to increase the absolute gate width without increasing the unit finger width is parallelize multiple transistor fingers. Fig. 6.3 shows the modelled noise parameters of 50 nm mHEMTs with a fixed absolute gate-width of 240 µm realized by the parallel connection of various finger numbers.

Realizing high absolute gate width by a high number of parallelized fingers improves T_{min}. R_n is almost constant (a slight improvement) when increasing the number of gate fingers. The phase of Γ_{opt} stays approximately constant since the absolute input capacitance is approximately constant for a constant absolute gate width. Devices with higher finger numbers have their Γ_{opt} positioned closer to the border of the Smith chart, which follows from the lower input resistance. This slightly hardens noise matching since the transformation to the 50 Ohm admittance circle is larger at the border of the Smith chart. This sets additional constraints for broadband matching and stability. The number of parallelized gate finger cannot be chosen arbitrarily high in the frequency regime of interest since devices are hard to embed into the given on-chip waveguide structures and tend to behave non ideal, which has been observed by several groups [6.12, 6.13]. This demands for a trade between lower device T_{min} of highly parallelized HEMTs and the ability to achieve broadband matching and stability more easily with a lower amount of parallelization.

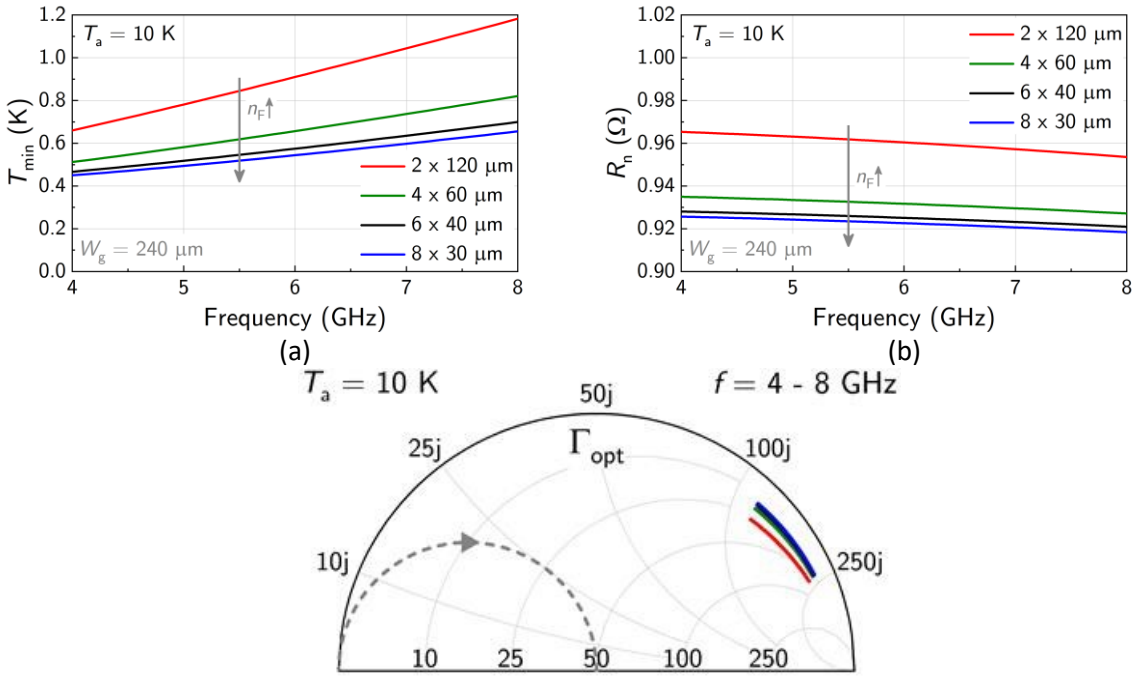


Fig. 6.3. Modelled noise parameters of 50 nm mHEMT devices with a fixed absolute gate-width of W_g = 240 µm operated at 10 K and biased at V_d = 0.3 V and I_d = 50 mA/mm. The number of gate fingers is varied from two to eight while the absolute gate width is kept constant at W_g = 240 µm. The (a) minimum noise temperature T_{min}, (b) optimal source reflection coefficient Γ_{opt}, and (c) equivalent noise resistance R_n is depicted. HEMTs with two (red), four (green), six (black), and eight (blue) parallel gate fingers are shown.

Furthermore, the absolute current that is needed to achieve a certain gain increases approximately linearly with the absolute device gate width (see Fig. 6.2 (d), MSG is almost constant for different absolute gate width). Therefore, the power consumption increases, which is bad for scaling

qubit read-out amplifiers to very high numbers since the cooling power of the 4 K stage is limited. Additionally, higher DC power consumption can heat the chip and consequently degrade the LNAs noise performance.

A lower absolute gate width device needs a series inductance to transform Γ_{opt} to the 50 Ohm admittance circle in the Smith chart. As already mentioned, this adds losses at the input of the active device and increases its T_{min}. The larger the inductance needed the larger the losses and the degradation of the noise temperature.

These conflictive constraints demand for a trade-off regarding the transistor device size and geometry. Dependent on the DC power levels that can be accepted and the noise temperatures target different device sized might be optimal. The model analysis provided in this report has been used extensively in Workpackage 3 to design the cryogenic C-band read-out LNA MMICs.

For the sake of better comparability and simplicity, the analysis provided above is given for common-source HEMTs only. In an LNA, simultaneous power and noise matching needs to be achieved, which is commonly realized by inductive source degeneration. The technique allows to tweak S_{11} without having a significant impact on the Γ_{opt} transformations discussed before. The source inductance adds some losses and degrades the device T_{min}. Similar to Γ_{opt} the amount of source inductance needed for proper matching is dependent on the device geometry and therefore, it needs to be taken into account simultaneously.

A detailed investigation on the basis of accurate model data - as provided above - is essential to design high-performance cryogenic ultra-low-noise amplifiers. The highly scalable and temperature dependent small-signal and noise model for HEMTs developed and extracted at Fraunhofer IAF enables such an analysis. Especially the accurate description of the scalability of the active devices and the ability to precisely predict their electrical behaviour at cryogenic temperatures are keys to fine tune LNA designs dedicated to cryogenic operation. The method has been applied successfully to actual cryogenic LNA design, which is reported by Fraunhofer IAF in Workpackage 3. The fabrication and measurement of the actual LNA MMICs verifies the model investigations provided in this report.

7 RF parameter extraction in 22nm FDSOI devices at cryogenic temperatures (contributor: EPFL)

7.1 Introduction

In the recent years, the cryogenic DC operation of some advanced silicon technologies has been studied mainly for quantum computing applications [7.1-7.5]. It shed more light on how threshold voltage, subthreshold swing, and mobility change for a transistor operating at cryogenic temperatures. It allowed the implementation of DC building blocks at low temperatures. On the other hand, the RF circuit is also a key building block in a quantum processor. For instance, the low-noise amplifier (LNA) used for RF reflectometry operates at a frequency around a few GHz. However, the RF behavior of some advanced technologies has not been fully addressed yet [7.6-7.7]. Additionally, the industrial 22 nm FDSOI technology has been used to implement a CMOS spin qubit due to its ultra-thin channel silicon-on-insulation (SOI) structure [7.8-7.10]. The advanced FDSOI technology can potentially be adopted for the monolithically integration of the quantum processor together with the read-out electronics. Thus, the RF modeling of an industrial 22 nm FDSOI technology is studied in this section.

7.2 RF modeling for a 22 nm FDSOI technology

This section discusses two analytical RF models. The first one was built initially for bulk technologies accounting for two current sources controlled by gate and source voltage [7.11]. The second model improves the first one by having the voltage-controlled current source (VCCS) from the back gate, which is more dedicated to the FDSOI MOSFET with a thin buried oxide layer (BOX). The two models are addressed correspondingly.

7.2.1 Model 1

Figure 7.1 shows the equivalent small-signal model on top of the cross-section of an FDSOI MOSFET. Due to the mentioned fact that such model was originally developed for bulk technologies, it only considers the VCCS, I_m and I_{ms}. Since in EKV the bulk is taken as a voltage reference, the back-gate VCCS I_{mb} is simply not considered. Moreover, the capacitances C_{BD} and C_{BS} originally represent the junction capacitances between the substrate and drain and substrate and source, respectively. But in an FDSOI MOSFET, the terms C_{BD} and C_{BS} represent the dielectric capacitances

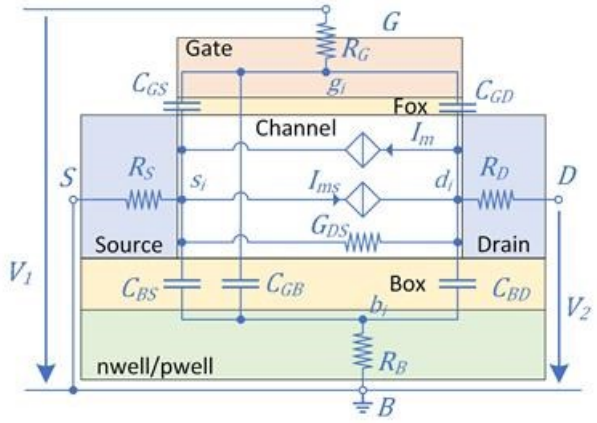


Fig. 7.1. *The equivalent small-signal model accounting for a simple substrate network and two VCCS, I_m and I_{ms}.*

due to the BOX, which is around 20 nm [7.12]. The substrate resistance R_B models the substrate.

Although a very simple model for such a complex FDSOI technology, we will see that it can do already a good job.

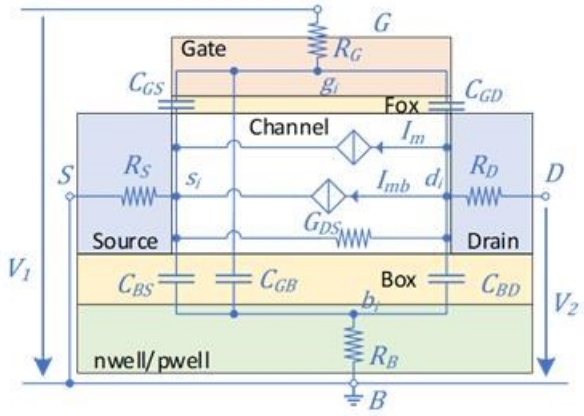


***Fig. 7.2**. The equivalent small-signal model accounting for a simple substrate network and two VCCS, I_m and I_{mb}.*

The equivalent small-signal circuit shown in Fig. 7.2 results in the analytical Y-parameters by ignoring the access resistances and the high-order components, given as

$$\boldsymbol{Y} = \begin{bmatrix} 0 & 0 \\ G_m & G_{DS} \end{bmatrix} + \omega^2 \boldsymbol{A} + i\omega \boldsymbol{B}. \tag{7.1}$$

The analytical Y-parameters consist of DC, frequency-dependent real and imaginary parts. The frequency-dependent real part is proportional to ω^2 with the coefficient matrix $\boldsymbol{A}$, represented by

$$\begin{aligned} A_{11} &\approx \omega^2 (C_{GB}^2 R_B + C_{GG}^2 R_G) \\ A_{12} &\approx \omega^2 (C_{BD} C_{GB} R_B - C_{GD} C_{GG} R_G) \\ A_{21} &\approx C_{GB} R_B (C_{BD} - C_m + C_{ms}) - C_{GG} R_G (C_{GD} + C_m) \\ A_{22} &\approx C_{BD} R_B (C_{BD} - C_m + C_{ms}) + C_{GD} R_G (C_{GD} + C_m) \end{aligned} \tag{7.2}$$

The imaginary part of analytical Y-parameters is proportional to ω with the coefficient matrix $\boldsymbol{B}$

$$\begin{aligned} B_{11} &\approx C_{GG} \\ B_{12} &\approx -C_{GD} \\ B_{21} &\approx -C_{GD} - C_m \\ B_{22} &\approx C_{BD} + C_{GD} \end{aligned} \tag{7.3}$$

7.2.2 Model 2

Model 2 improves Model 1 by considering the back-gate VCCS I_{mb} as shown in Fig. 7.2. Besides, in advanced silicon technologies with high-κ front-gate implementation, the front-gate resistance R_G shows a higher value than that in conventional technologies. Model 2 hence keeps the contribution of R_G and R_B in the imaginary part of Y_{21} and Y_{22}. It should be noted that back-gate transconductance G_{mb} is relatively small compared to G_m by typically a factor of 20 due to the 20 nm thick BOX layer. Therefore, the term G_{mb} can finally be neglected in the model. Consequently, the updated equivalent small-signal circuit has the same format as Eq. (7.1) but with matrix $\boldsymbol{A}$, given as

$$\begin{aligned} A_{11} &\approx \omega^2 (C_{GB}^2 R_B + C_{GG}^2 R_G) \\ A_{12} &\approx \omega^2 (C_{BD} C_{GB} R_B - C_{GD} C_{GG} R_G) \end{aligned} \tag{7.4}$$

$$A_{21} \approx C_{GB}R_B(C_{BD} + C_{mb}) - C_{GG}R_G(C_{GD} + C_m)$$
$$A_{22} \approx C_{BD}R_B(C_{BD} + C_{mb}) + C_{GD}R_G(C_{GD} + C_m)$$

and matrix $\boldsymbol{B}$ is expressed as

$$\begin{aligned} B_{11} &\approx C_{GG} \\ B_{12} &\approx -C_{GD} \\ B_{21} &\approx -C_{GD} - C_m - C_{GG}G_mR_G \\ B_{22} &\approx C_{BD} + C_{GD} + C_{GD}G_mR_G \end{aligned} \tag{7.5}$$

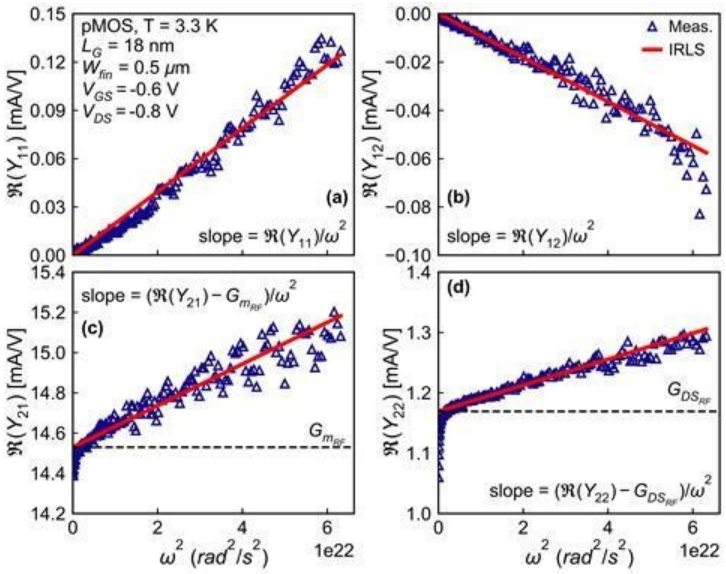


Fig. 7.3. *The application of iteratively reweighted least squares for extracting the slope of real-part Y versus* ω^2.

7.3 Experimental validation

This section addresses the extraction methodology and experimental validation for the corresponding models.

7.3.1 Model 1

The extraction methodology for Model 1 follows the steps:

1. De-embedding the DUT signal by the open and short structure at each temperature.
2. Extracting the capacitances from the imaginary part of the Y-parameters.
3. Extracting the matrix $\boldsymbol{A}$ (Eq. (7.2)) from the real part of Y-parameters by using iteratively reweighted least squares (IRLS).
4. Computing the remaining parameters analytically from matrix $\boldsymbol{A}$.

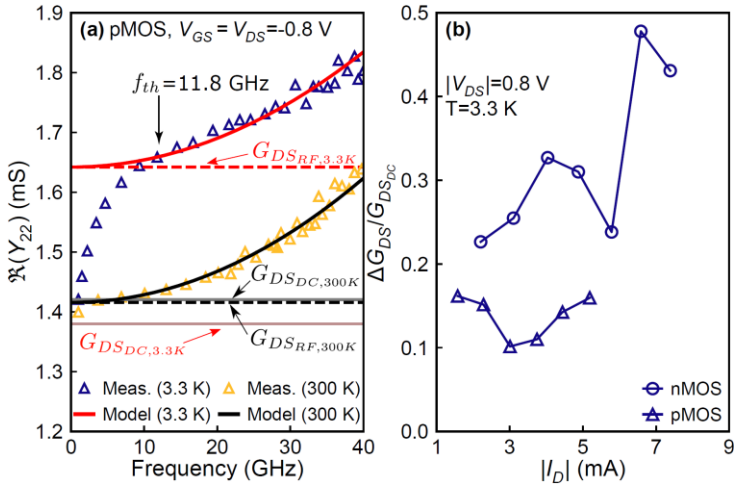


***Fig. 7.4**. Dynamic self-heating effect in $\Re(Y_{22})$, which shows a drop in few-GHz regime.*

In the third step, the iteratively reweighted least squares (IRLS) method is adopted for extracting the matrix $\boldsymbol{A}$ from the real-part Y versus ω^2. The least squares method measures the slope of the linear trend as shown in the real-part Y versus ω^2. Unlike the regular least-squares method, IRLS automatically screens out the outliers and non-quadratic components, e.g., self-heating, as shown in Fig. 7.3. For instance, $\Re(Y_{22})$ shows a strong drop at a few GHz frequencies at 3.3 K due to the dynamic self-heating effect, which is not quadratic as the model describes. Even though the IRLS regression line successfully captures the slope of the experimental data with an extrapolation of $G_{DS_{RF}}$ at static regime. The application of IRLS allows the robust automated extraction for the data, including the self-heating effect. Otherwise, a frequency boundary for filtering outliers should be given manually. Consequently, in Fig. 7.4, the analytical model of $\Re(Y_{22})$ has a nice agreement with measurement at 300 K and 3.3 K. In particular, comparing experimental $\Re(Y_{22})$ with model leads to a thermal cut-off frequency f_{th}, which is the critical parameter for the associated thermal network. If the signal is above such frequency, the dynamic self-heating effect disappears due to the slow thermal response from the crystal. For instance, f_{th} is 11.8 GHz for a pMOS FDSOI at 3.3 K. On top of that, the dynamic self-heating effect results in ΔG_{DS}, which is the difference between $G_{DS_{DC}}$ and $G_{DS_{RF}}$. Fig. 7.4 (b) further presents the self-heating influence for nMOS and pMOS at 3.3 K by showing $\Delta G_{DS}/G_{DS_{DC}}$ versus drain current. In such measurement, the self-heating effect is more pronounced for an nMOS device, where the larger drain current leads to the high $\Delta G_{DS}/G_{DS_{DC}}$.

Once the matrix $\boldsymbol{A}$ is extracted, the remaining parameters are computed analytically. Fig. 7.5 shows the validation of Model 1 through the experimental Y-parameters at 300 K and 3.3 K. Both real and imaginary Y-parameters models compare well to the measurement. It should be noted that the contribution of R_B is experimentally found small at low temperatures, and hence the term R_B in the small-signal circuit is set to 0 Ω. It results in a room-temperature model and a low-temperature model; the former has R_B accounting for substrate network, the latter one does not have R_B.

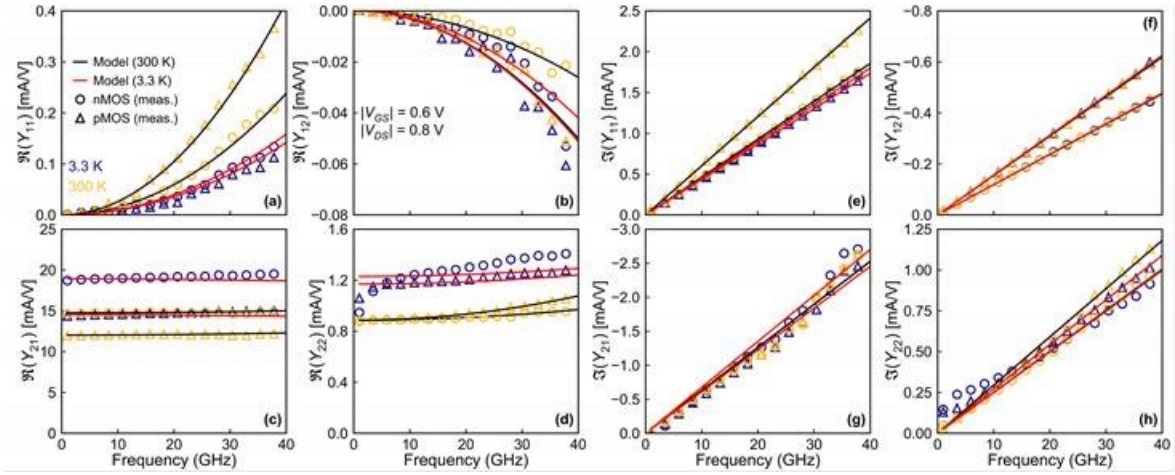


Fig. 7.5. The experimental validation to Model 1 at room temperature and at 3.3 K.

7.3.2 Model 2

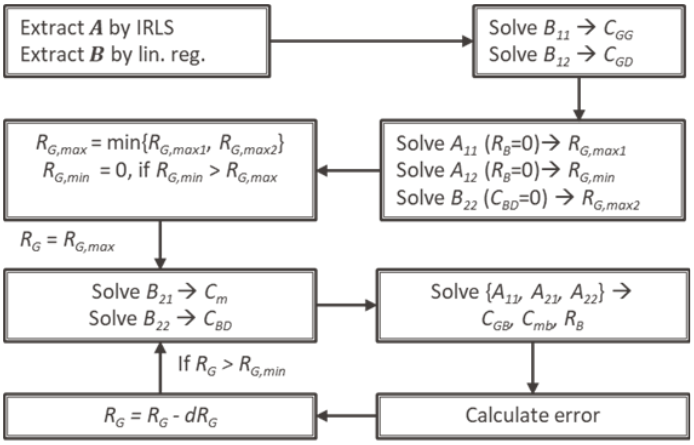


Fig. 7.6. *The extraction flow for Model 2.*

Unfortunately, Model 2 does not have the analytical solution by solving Eq. (7.4) and (7.5). Moreover, we learned that the influence of R_B fading at low temperature is actually because of decreasing C_{GB} and C_{BD}. Therefore, the dedicated extraction flow is introduced in Fig. 7.6 while keeping all parameters during the extraction. The proposed extraction flow looks for a pair of parameters with a minimum error in a specific range. First, the matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ are extracted from the de-embedded DUT Y-parameters; the former by the IRLS method and the latter by a regular linear regression. Second, C_{GG} and C_{BD} are extracted from B_{11} and B_{12}, respectively, and they are kept constant over the extraction. Due to the fact that the product $C_{GB}R_B$ and $C_{BD}R_B$ are relatively small compared to the products with R_G, the boundary of R_G is therefore defined through A_{11}, A_{12}, and B_{22} by assuming C_{BD} and R_B are zero. Third, once the boundary of R_G is fixed, the extraction loop starts with the maximum R_G and stops at the minimum R_G. Each R_G value leads to remaining parameters by solving the corresponding equations. Finally, the error is computed by comparing the modeled matrix $\boldsymbol{A}$ and experiments.

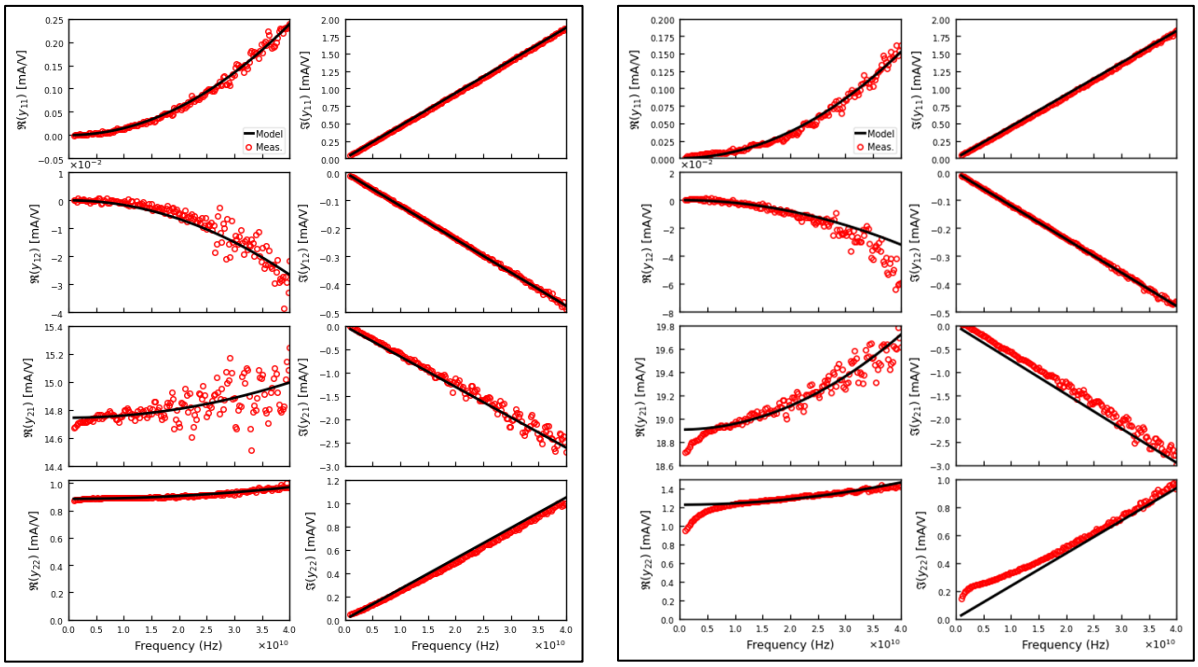


Fig. 7.7. *Experimental validation of Model 2 through the Y-parameters of an nMOS with 18 nm gate length at 300 K (a) and 3.3 K (b) and at $V_G = 0.6$ V and $V_D = 0.8$ V.*

Fig. 7.7 presents the model validation for an nMOS at 300 K and 3.3 K. The analytical model with extracted parameters compares very well to the measurement over a large temperature range. The extracted parameters are shown for each temperature in Fig. 7.8.

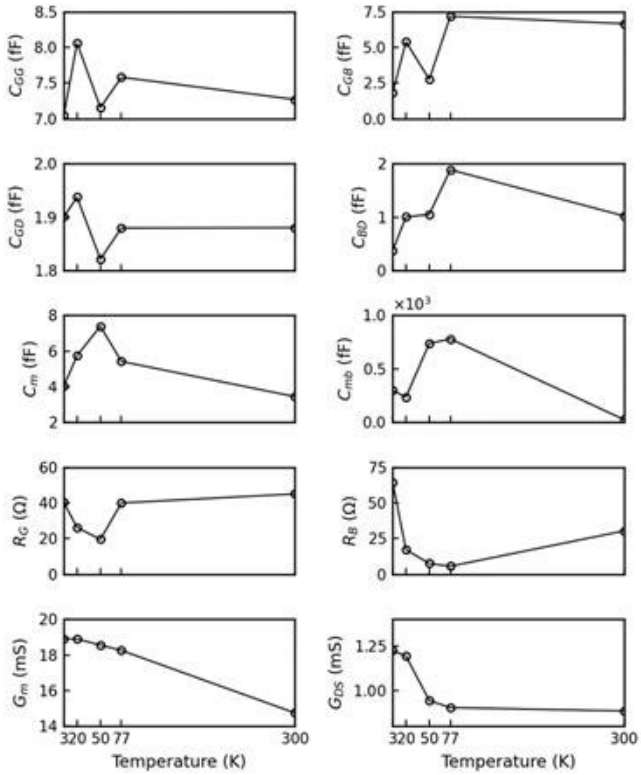


Fig. 7.8. *Model 2 parameters over temperature.*

The terms C_{GG} and C_{GD} are almost constant with respect to temperature. On the other hand, C_{GB} and C_{BD} get smaller as temperature decreases, which is the reason that the R_B contribution is diluted at low temperatures. In fact, since dopants are incompletely ionized at low temperatures, R_B rises significantly below 50 K.

The term C_m and C_{mb} are accounted in the VCCS from front-gate and back-gate separately, given as

$$\begin{aligned} I_m &= G_m\left(1 - i\omega\tau_{qs1}\right)V_{GS} = (G_m - i\omega C_m)V_{GS} \\ I_{mb} &= G_{mb}\left(1 - i\omega\tau_{qs2}\right)V_{BS} = (G_{mb} - i\omega C_{mb})V_{BS} \end{aligned} \tag{7.6}$$

According to Fig. 7.8, C_{mb} is larger than C_m by around two orders. This implies that the quasi-static time constant τ_{qs} from the back gate is much larger than that from the front gate while $G_m \gg G_{mb}$. Such experimental finding is because BOX is around 20 times thicker than effective front dielectric thickness.

8 LF noise characterization of vertical III-V NW MOSFETs at cryogenic temperatures (contributor: ULUND)

8.1 Introduction

LFN is widely used as a technology quality metric for transistors to evaluate material quality as well as transport properties. To address the lack of LFN characterization at cryogenic temperatures, recently, cryogenic 1/f characterization for fully-depleted silicon-on-insulator (FDSOI) MOSFETs was reported [8.1]. There have been reports on LFN for III-V nanowire MOSFETs at room temperature, but to the best of our knowledge, none yet at cryogenic temperatures [8.3-8.6]. Here, we present low-frequency noise characterization at temperatures down to 15 K. We observe that the dominant mechanism of 1/f-noise in vertical InAs/InGaAs GAA MOSFETs changes from border and interface trap induced number fluctuations to mobility fluctuations originating from the nanowire core.

8.2 Device fabrication

A cross-sectional illustration and a scanning-electron-microscope (SEM) image of the fabricated III-V vertical GAA MOSFET with gate length (L_G) of 70-nm and gate width (W_{NW}) of 27-nm is shown in Fig. 8.1. The process starts by first growing a 300-nm-thick InAs buffer layer on a Si substrate. The vertical nanowires are then grown by Vapor-Liquid-Solid (VLS) growth where electron beam lithography (EBL) patterned Au seed particles are used as nanowire nucleation sites. A similar growth scheme was implemented in [8.7]. The drain top metal-contact height is defined by first spin coating a hydrogen silsesquioxane (HSQ) film and then by using EBL. The drain contact is made up of 20-nm-thick Mo and 1.5-nm-thick TiN that are anisotropically etched away on the horizontal surface using reactive-ion-etching (RIE) so that the metal only remains on the vertical nanowire sidewalls. The HSQ layer is then etched away using a buffered-oxide-etch (BOE) solution.

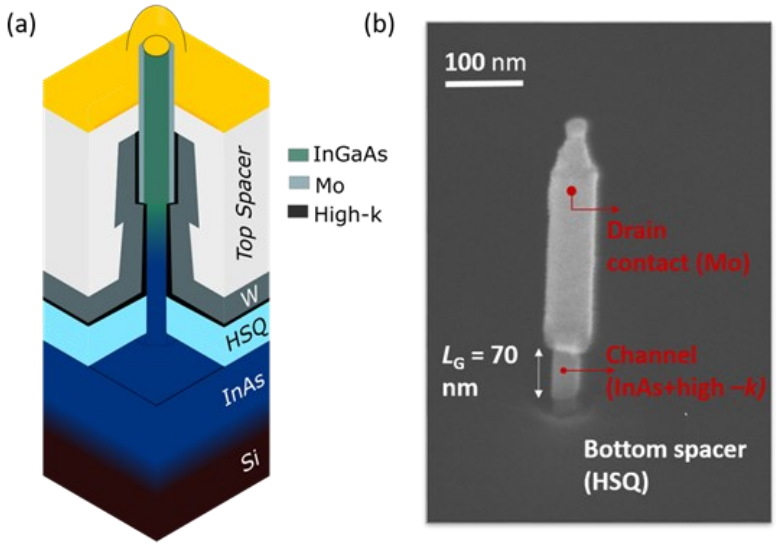


Fig. 8.1. *(a) Cross-sectional illustration of a vertical InAs/InGaAs GAA MOSFET showing the different contacts and separation layers (b) A SEM image of the InAs/InGaAs vertical GAA MOSFET with L_G = 70-nm and W_{NW} = 27-nm post gate dielectric deposition.*

A gate length of 70-nm is defined using a gate-last process [8.8]. The doped shell around the channel is removed using a digital etch process in which the shell is oxidized using ozone and then etched in a HCl:IPA solution. For the gate dielectric, an Al_2O_3/HfO_2 bilayer was deposited using ALD which resulted in an EOT of 1.5-nm. The gate-metal comprising of a 2-nm-thick TiN and 60-nm-thick W is deposited using ALD and sputtering. The fabrication is then completed by depositing a top spacer layer, etching vias to contacts and final metallization using Ni/Au contacts (10-nm/100-nm).

8.3 Electrical characterization and analysis

DC characterization of the vertical InAs/InGaAs GAA MOSFETs was performed with an Agilent B1500 parameter analyzer. Fig. 8.2(a) and Fig. 8.2(b) show the output characteristics at room temperature and transfer characteristics with temperatures ranging from 300 K to 15 K, respectively, for the vertical InAs/InGaAs GAA MOSFET. A V_{DS} of 50 mV to measure the transfer characteristics was chosen as it is a typical bias for low-frequency noise measurements [8.1,8.4,8.5]. With decreasing T, the absolute value of the threshold voltage (V_{TH}) shifts towards higher values by ≈ 0.5 mV/K (Fig. 8.2(c)) which is comparable to Si n-channel MOSFETs and an improvement over previously reported InAs/HfO_2 nanowire MOSFETs [8.1-8.3]. Fig. 8.2(d) shows the inverse subthreshold slope (SS), $\partial V_{GS}/\partial(\log I_{DS})$ as a function of I_{DS} for four temperatures. It can be noted that the SS decreases to 36 mV/dec at 15 K at which the LFN characterization is performed.

For the LFN measurements, a low-noise preamplifier was used to supply a constant V_{DS} = 50 mV and the current noise power spectral density (PSD) was measured using a lock-in amplifier. A similar setup was used in our previous LFN reports [8.4-8.6]. The frequency was swept between 1 Hz and 1 KHz and the temperature was varied from 300 K to 15 K. At every temperature point, a gate voltage (V_{GS}) was applied so that the overdrive voltage ($V_{OD} = V_{GS} - V_{TH}$) was zero [8.1].

The 1/f-noise behavior for different temperatures are shown in Fig. 8.3(a). Although, no strong temperature dependence on LFN magnitude was observed, it can be confirmed that the measured drain current noise spectral density (S_{ID}) has a typical $1/f^{\gamma}$ dependency at all measured temperatures with γ ranging from 0.8 to 1.1.

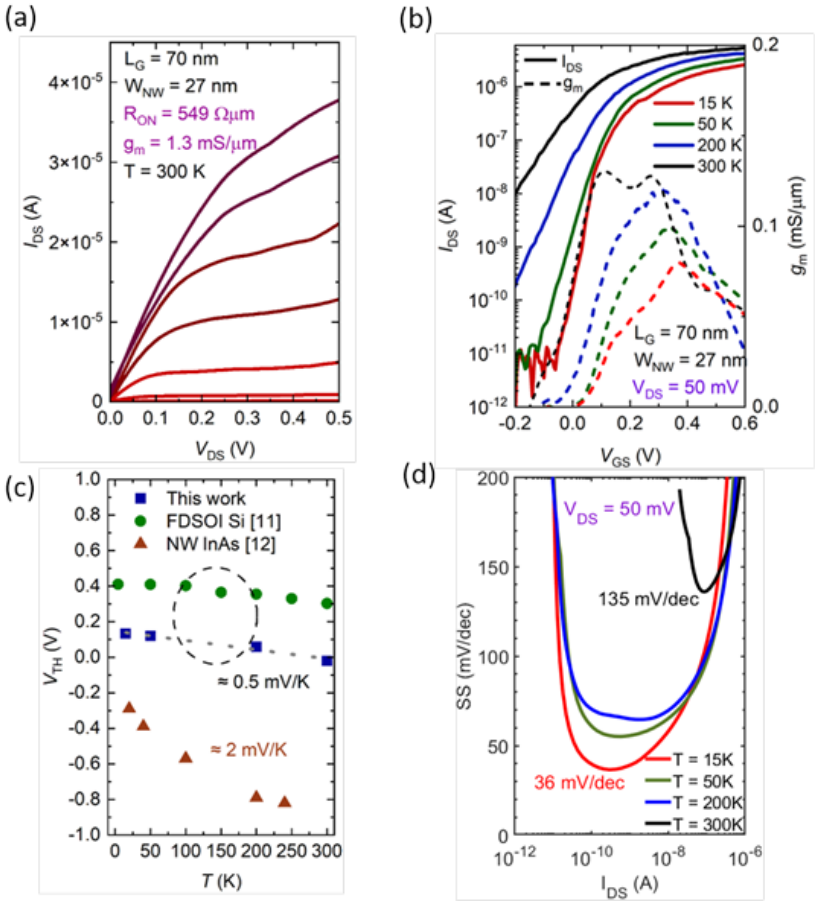


***Fig. 8.2**. (a) Output characteristics at 300 K for a vertical InAs/InGaAs GAA MOSFET with R_{ON} = 549 Ωμm and g_m = 1.3 mS/μm at V_{DS} = 0.5 V and (b) Transfer characteristics measured at different temperatures with V_{DS} = 50 mV (c) V_{TH} versus T and (d) Inverse subthreshold slope versus T at V_{DS} = 50 mV for an InAs/InGaAs NW MOSFET.*

The two mechanisms that generally explain the LFN in MOSFETs are carrier number fluctuations (CNF) and mobility fluctuations (MF). CNF arise from border traps present in the gate dielectric, whereas MF are caused due to electron-phonon scattering within the channel often described with the material dependent Hooge model. The mechanisms can be identified by measuring the drain current noise spectral density (S_{ID}) as a function of drain current (I_{DS}). When S_{ID}/I_{DS}^2 is proportional to $1/I_{DS}$, the LFN is expected to originate from MF. Instead, when S_{ID}/I_{DS}^2 is proportional to the trans-conductance squared (g_m^2/ I_{DS}^2), the LFN is expected to arise from CNF [8.9]. To identify the noise mechanism in InAs/InGaAs vertical GAA MOSFETs, extended measurements were carried out at a frequency of 10 Hz. Interestingly, it can be noted from Fig. 8.3(b) that the mechanism of LFN in InAs/InGaAs vertical GAA MOSFETs changes from carrier number fluctuations to mobility fluctuations when the temperature is reduced from 300 K to 15 K. This can be attributed to the current conduction being dominant at the nanowire surface at 300 K where the transport is more sensitive to charge trapping/de-trapping. On the other hand, when the temperature is reduced to 15 K, the conduction is mainly through the nanowire core due to the freezing out of the border traps. Notably, surface and core conduction modes were also previously observed at room temperature where the

III-V vertical GAA MOSFET showed core conduction when biased below V_{TH} and surface conduction above V_{TH} [8.6].

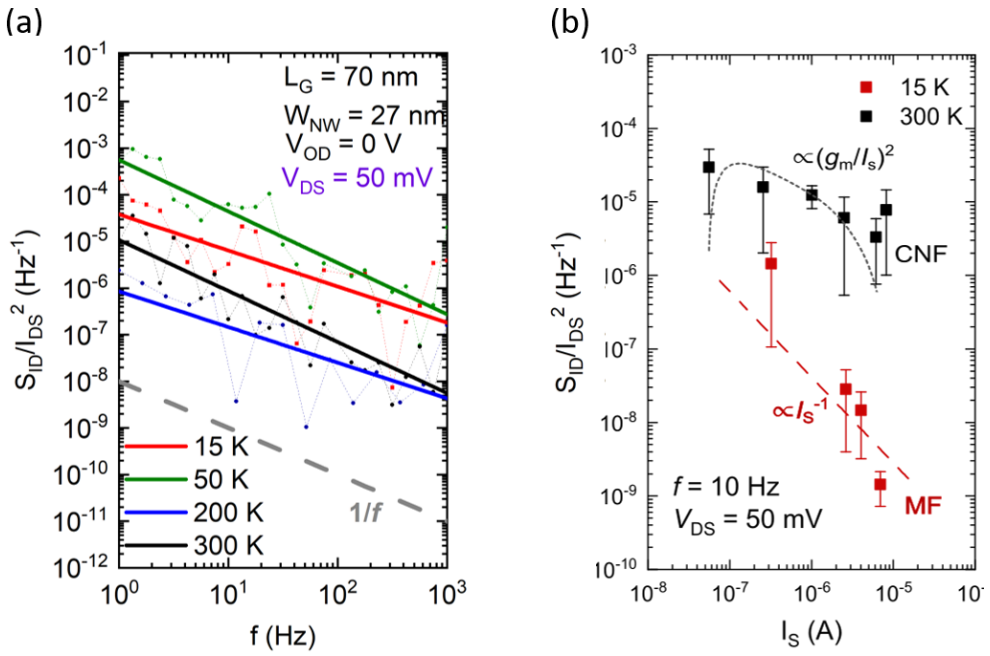


Fig. 8.3. *(a) Drain current noise spectral density (S_{ID}) plotted versus frequency at different temperatures for a InAs/InGaAs vertical GAA MOSFET (b) S_{ID}/I_S^2 measured at a fixed frequency of 10 Hz at T= 300 K and T = 15 K.*

Fig. 8.4 (a) shows the input-referred gate voltage noise spectral density (S_{VG}). It is a commonly used metric that represents the minimum signal amplitude that can be amplified by the transistor [8.4]. At cryogenic temperatures, when compared to 1–µm-long FDSOI MOSFETs measured at 4.2 K, the InAs/InGaAs vertical GAA MOSFETs have comparable SVG. The Hooge parameter (αH) at 15 K for the InAs/InGaAs vertical GAA MOSFETs having a gate width, WNW = 27-nm was calculated using (8.1) to be 5 × 10-6,

$$S_{ID}/I_{DS}^2 = q\mu_{eff}\alpha_H V_{DS}/L_G^2 f\, I_{DS} \quad (8.1)$$

where q is the elemental charge, μ_{eff} the effective channel mobility, and f the frequency.
From Fig. 8.4 (b), it can be noted that the Hooge Parameter at 15 K improves by at least a factor of 10 when compared to previously reported α_H values for various nanowire FET technologies at room temperature. The lowering of α_H indicates a reduction in electron-phonon scattering at lower temperatures that is advantageous for cryogenic applications. The minimum border trap density (N_{bt}) for the InAs/InGaAs vertical GAA MOSFET was determined as in ref. [8.6] to be 2×10^{19} cm^{-3} eV^{-1} which is not too far away from previously reported N_{bt} values for planar Si MOSFETs with HfO_2 gate oxides and a SiO_2 interface layer [8.4]. Our results indicate the InAs/InGaAs vertical GAA MOSFETs to be an attractive option to be used in emerging III-V cryogenic circuits.

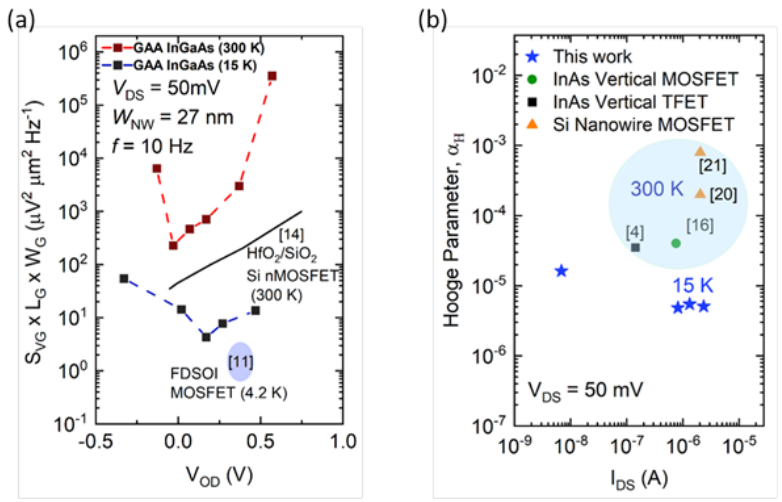


Fig. 8.4. *(a) Input referred voltage noise power spectral density (S_{VG}) normalized with the gate area. (b) Calculated Hooge parameter for InAs/InGaAs vertical GAA MOSFET at 15 K and other nanowire technologies at 300 K.*

9 Summary and conclusions

INPG/IBM have performed a detailed electrical characterization of scaled planar InGaAs-on-Silicon MOSFETs from room temperature down to deep cryogenic temperatures (10K). The main MOSFET parameters (threshold voltage V_t, low-field mobility μ_0, and subthreshold swing, SS) were extracted in linear region of operation using the consolidated Y-function method for gate lengths down to 10 nm, despite the possible presence of L-valley conduction, and were benchmarked to Si CMOS. The results build on the understanding of the operation of cryogenic III-V MOSFETs and indicate that this technology may be promising for future low-power cryogenic quantum computer applications. The saturation velocity was also extracted and analysed for all lengths and temperatures. The extracted parameters of the III-V devices follow the expected behavior with temperature as in Si, while demonstrating competing advantages as compared to Si MOSFETs, particularly when going down to cryogenic temperatures. However, the low frequency noise performances of III-V MOSFETs have been found one to two orders of magnitude lower than in 22nmFDSOI MOS devices.

INPG/LETI have carried out a detailed electrical characterization and transistor parameter extraction on 200mm CMOS compatible GaN/Si HEMTs down to deep cryogenic temperatures. The main transistor parameters (threshold voltage V_{th}, low-field mobility μ_0, and subthreshold swing, SS, R_{sd}) were extracted in linear region (V_d=50mV) using the Y-function and the Lambert-W function methods for gate lengths from 3µm down to 0.1µm. The Y-function method was also employed in saturation region (V_d=5V) for the extraction of the saturation velocity. The results indicate that those 200mm CMOS compatible Ga/Si HEMT devices show a very good functionality down to very low temperature (10K) with significant improvement of mobility and subthreshold slope. In long channels, the low field mobility μ_0 is found to increase from 2000 cm^2/Vs up to 4000 cm^2/Vs from 300K down to 10K due to phonon scattering reduction. In contrast, in short devices, the low field mobility is nearly temperature independent likely due to neutral defect scattering dominance. The saturation velocity v_{sat} is found to overcome $10^7 cm/s$ at low temperature. The source-drain series resistance R_{sd} is shown by TLM analysis to be more controlled by the contact resistance R_c than the 2DEG access region resistance as the temperature is decreased. Finally, it is worth noting that the Lambert-W function modelling of the drain current characteristics could constitute a simple compact model for such GaN/Si HEMTs down to deep cryogenic conditions, as is the case in Si MOSFETs.

Moreover, **INPG/IBM** have performed a thorough experimental analysis of novel InGaAs-based HEMT devices down to 10K, within the framework of technologies for quantum computing. The onset of conduction in satellite valleys, demonstrated for the first time owing to g_m and Y-function analysis, can motivate possible process optimization of the InGaAs alloy so to push it to higher gate bias. The InGaAs devices were found to preserve their high mobility and output current, while simultaneously performing similarly or even better than mature Si technologies (FDSOI), in terms of self-heating and low-frequency noise, thanks to the bulk-like InAlAs/InGaAs heterostructure. This HEMT technology is therefore highly promising for cryogenic electronics, particularly for future qubit readout LNAs in quantum computing.

Fraunhofer IAF has developed and extracted a highly scalable small-signal and noise model for 50 nm mHEMTs that is valid down to cryogenic temperatures throughout the project. This accurate model is used to perform a detailed analysis on how the noise performance of cryogenic HEMT LNA MMICs can be further improved by circuit design techniques. An extensive analysis on how the choice of the device geometry in terms of gate width influences the noise performance at cryogenic temperature and resulting implications on the input matching network has been given. Other rele-

vant LNA characteristics as input power matching, gain, DC-power consumption und size are also tackled by the investigation. The methods described have been used in Workpackage 3 for cryogenic LNA design and the results shown proof the validity of the model and the method.

EPFL has developed an analytical RF FDSOI model owing to the analytical study on the RF signal of nMOS/pMOS FDSOI from room temperature down to 3.3 K,. Model 1 and Model 2 have been validated down to low temperatures. The former model was originally for bulk technology. The latter is hence introduced to better meet with the FDSOI configuration. Particularly, the current source controlled by the back-gate voltage is included. Besides, the extracted parameters based on Model 2 show that the contribution of R_B to the Y-parameters is diluted at low temperatures due to the decrease of C_{GB} and C_{BD}. Finally, it is experimentally found that C_{mb} is around two orders larger than C_m, which suggests the intrinsic quasi-static time constant of the back gate is much larger than that of the front gate. This finding, which is not discussed yet in the literature, is ascribed to the fact that BOX is much thicker than the front dielectric.

Tyndall's multi-frequency C-V experimental data recorded at low temperature confirm phonon assisted tunnelling process as the main emission and capture process of carriers from and into the oxide defects. The two dielectrics investigated present parallel behaviour: at 10 K, the dispersion in n-MOScaps is fully suppressed while in p-MOScaps it is still significantly present. The space and energy profiling of oxide traps using physics based simulations was successful from room temperature down to -50°C. More effort is underway to exploit the electrical characteristics at extended temperature range (below -50°C).

ULUND have studied the cryogenic 1/*f*-noise behavior in a InAs/InGaAs vertical GAA MOSFET. At 300K, it has been observed that carrier number fluctuations are the dominant source of LFN resulting from the dielectric border traps. Whereas, at 15 K, the conduction is less surface sensitive and the LFN is dominated by mobility fluctuations having a low $\alpha_H = 5 \times 10^{-6}$. Although III-V MOSFETs have been recently implemented in cryogenic applications, there is a lack of cryogenic low-frequency noise characterization for the same. Therefore these experimental results can contribute to III-V nanowire MOSFET design aimed towards low temperature applications.

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