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1 Introduction

The SEQUENCE project offers a unique opportunity to perform characterization and modeling of various Si and III-V devices and use them in electronics for quantum computing and communication applications. This specific effort within SEQUENCE covers the modeling of a) new effects appearing in devices operating at low temperature in order to better understand the physics that governs these phenomena, b) the compact modeling of such phenomena so that they can be embedded in compact models available for the design and c) simplified models that can help the circuit designers in better sizing their circuit to optimize their performance at low temperature. A good example is the modeling of the saturation of the subthreshold swing that is observed at low temperature. It was first characterized experimentally [1] and modelled using a physics based model [1] [2] and finally a physics-based empirical model that is simple enough to include in a compact model [3]. Now, a compact model would be useless without clear parameter extraction procedures.

Compact semiconductor models (CM) are the link between the newly developed technologies or the new use of existing technologies (at cryogenic temperature for example) and the environment enabling the design of circuits. This is why they are essential to make these new technologies or their new use accessible to the designers. Although CM for existing CMOS technologies such as bulk, FDSOI or FinFET are rather mature for use at room temperature, they break down when used at cryogenic temperatures.This is why it is essential to develop new models or update existing ones so that they are also valid at cryogenic temperatures.

This report describes the results obtained within the SEQUENCE for the development of such CM for various technologies, mature CMOS technologies and other technologies under development. It starts with a description of the recent progress made in the extraction tool developed by EPFL to extract the parameters of the EKV CM in a fully automatic way. The extractor is based on python and is made available to all the SEQUENCE partners. The first RF measurements made on a 22 nm FDSOI process at 3.3 K are then presented.

INPG and LETI are then presenting how the Lambert-W function can be used for modeling FDSOI devices at cryogenic temperature. It is then shown how the Kubo-Greenwood formalism can be applied to FDSOI MOSFETs operating at cryogenic temperature.

Fraunhofer IAF then report on a scalable small-signal and noise model of a 50 nm metamorphic high-electron-mobility transistor (mHEMT) technology dedicated to high performance cryogenic circuit design. The model is continuously valid down to cryogenic temperatures and up to high frequencies. The proposed model provides the designer a high flexibility in the design of RF circuits.

Finally, ULUND presents a model of band tails that uses an extension of the density of states utilizing generalized Fermi-Dirac integrals. This allows for a smooth transition between the exponentially decaying DOS below the mobility edge and linearly increasing DOS above.

The report finally ends with a summary and conclusions.

2 Simplified EKV modeling of advanced CMOS technologies and RF characterization down to cryogenic temperatures (EPFL)

This section presents an extensive characterization and simplified-EKV-based (sEKV) modeling of advanced CMOS technologies, from room temperature to cryogenic temperatures. Moreover, a Python-based extractor is developed to obtain sEKV parameters automatically. This programming project is versioned on GitLab [4], allowing the tool to be conveniently distributed among partners.

2.1 Model and extraction updates

The sEKV parameters extractor was already introduced in Deliverable D2.2. In the mean time the tool has been significantly enhanced and allows now full automatic extraction. The purpose of this section is to present those enhancements and improvements and the results obtained on various technologies.

2.1.1 Extraction methodology

Fig. 1 shows the extraction flow of the updated sEKV python-based automatic parameter extractor. First, transfer and output characteristics are converted into classes *IdVg* and *IdVd.* These classes have properties such as raw data, temperature, device geometry, etc. and they are passed to the block *sEKV extractor*. In addition, the subthreshold swing (SS) and the output conductance (G_{ds}) extraction modules have been developed; the former takes the *SS* saturation at cryogenic temperatures into account to estimate the region where SS is going to be extracted, and the latter extracts G_{ds} from the I_D-V_D characteristic for a given bias point or within a certain voltage range. It is worth noting that a Savitzky-Golay filter is applied to the SS extraction module to avoid fluctuations, which frequently happen at cryogenic temperatures because of low current level (i.e., pA) and resonant tunneling (Fig. 5).

2.1.2 Model of output conductance

The output conductance can be written by the chain rule as [5]:

$$G_{ds} \triangleq \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{\partial I_{DS}}{\partial V_T}\frac{\partial V_T}{\partial V_{DS}} = (-G_m)(-\sigma_d) \tag{1}$$

where $\partial I_{DS}/\partial V_T$ is equal to minus the transconductance ($-G_m$) and $\partial V_T/\partial V_{DS} \triangleq (-\sigma_d)$ describes the first-order approximation of the drain-induced barrier lowering (DIBL) effect, given by

$$V_T \cong V_{T0} - \sigma_d V_{DS}. \tag{2}$$

Consequently, there is a relation between G_{ds} and G_m given by

$$\frac{G_{ds}}{G_{spec}} \triangleq g_{ds} = \frac{\sigma_d}{n} g_{ms} \tag{3}$$

where the source transconductance ($G_{ms} = nG_m$) and G_{ds} are normalized by $G_{spec} = 2n\mu_0 C_{ox} U_T$ to be g_{ms} and g_{ds}, respectively. By expanding g_{ms} as a function of IC [6], we could finally have the expression of g_{ds} in terms of IC, given by

$$g_{ds} = \frac{\sigma_d}{n}\frac{\sqrt{(\lambda_d IC + 1)^2 + 4IC} - 1}{\lambda_d(\lambda_d IC + 1) + 2} \tag{4}$$

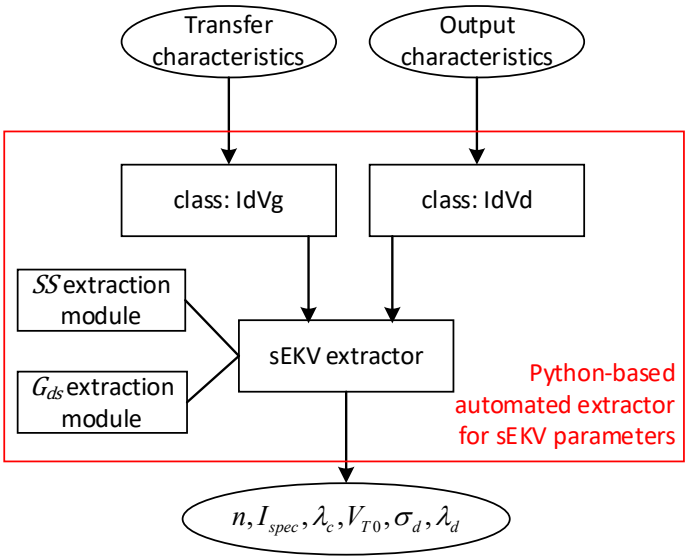


Fig. 1: Extraction flow of sEKV parameters, where extractor takes transfer and output characteristics as input variables and outputs six parameters.

where the parameter λ_c used for g_{ms} is replaced by λ_d because it has been obtained from the output characteristic. When IC is below 0.1 (in the weak inversion, WI), Eq. (3) is reduced to $g_{ds} = \sigma_d IC/n$. Hence, σ_d is extracted by doing linear regression on $\log g_{ds}$ versus $\log IC$ in the WI regime, as shown in Fig. 2. Finally, the residual parameter λ_d is optimized by applying non-linear regression. This results in a very good fit between measurments and model as demonstrated by Fig. 2.

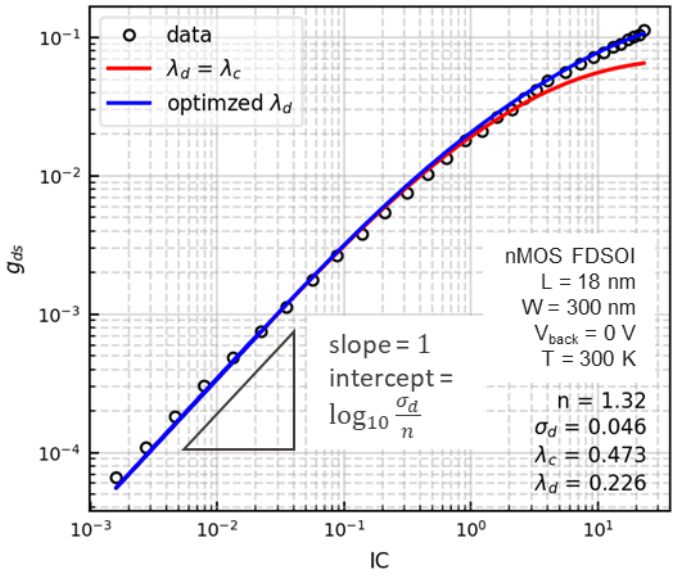


Fig. 2: normalized output conductance (g_{ds}) versus inversion coefficient (IC), where parameters σ_d and λ_d are extracted. The measurement is performed on nMOS FDSOI with W/L = 300 nm/ 18 nm at 300 K.

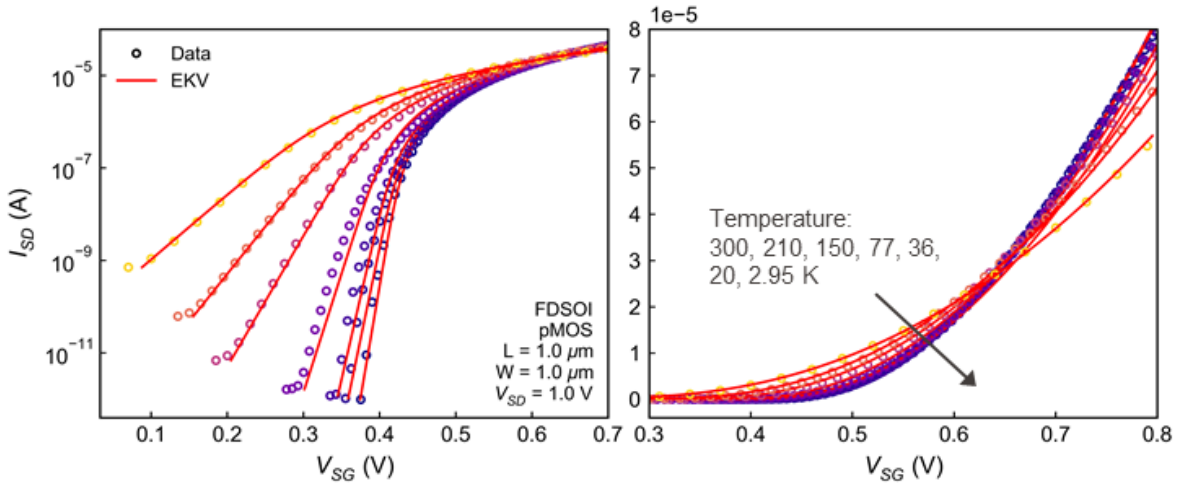


Fig. 3: EKV model validation of pMOS FDSOI with W/L = 1 µm/ 1 µm, which is measured at V_{SD} = 1 V, V_{back} = 0 V, and over a wide temperature range. (left) and (right) show the results in log and linear scales, respectively.

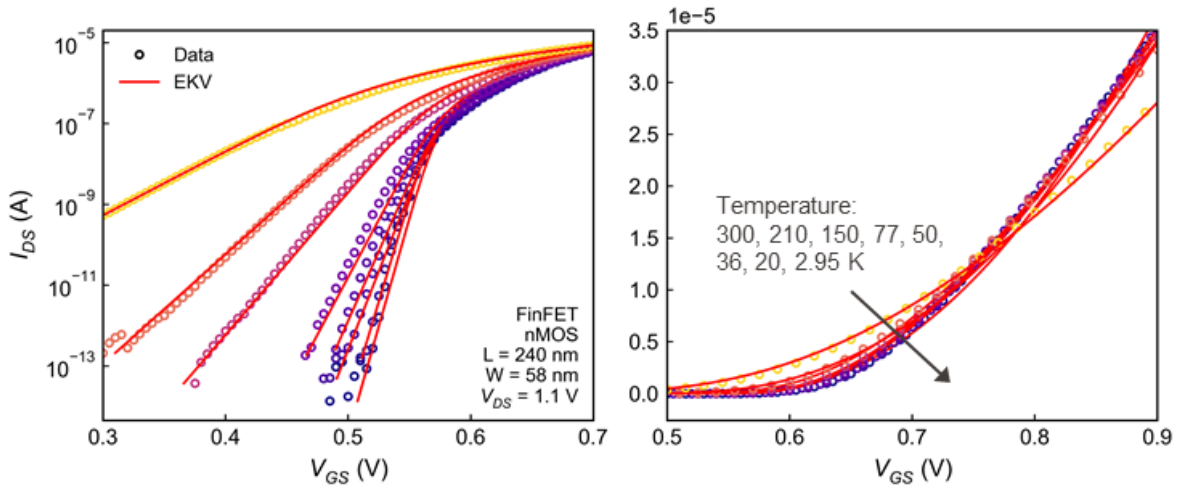


Fig. 4: EKV model validation of nMOS FinFET with W/L = 58 nm/ 240 nm, which is measured at V_{SD} = 1.1 V and over a wide temperature range. (left) and (right) show the results in log and linear scales, respectively.

2.2 Systematic validation of simplified EKV model (EPFL)

On top of the updated extractor addressed in Sec. 2.1, this section validates the sEKV model and automated extractor on advanced commercial CMOS technologies, including 16 nm FinFET and 22 nm FDSOI, from 300 K down to around 3 K.

2.2.1 Model validation with FinFET and FDSOI

Fig. 3 and Fig. 4 show the I_D-V_G of FinFET and FDSOI technologies with corresponding temperatures [7] [8]. We see that the automatic extractor provides a set of parameters leading to a very good agremment of the sEKV model to the measurements from room temperature down to cryogenic temperatures.

Thanks to the continuity of the sEKV model from weak to strong inversion, features like the exponential (below V_T) and the quadratic/linear I_D-V_G (above V_T) can be captured; therefore, the sEKV model can be widely applied to devices with planar or three-dimensional structures. It is worth noting that the sEKV model is developed from the conventional CMOS structure, i.e., bulk structure but it still applies for other technologies. However, the correction on charge distribution that is due to the strong

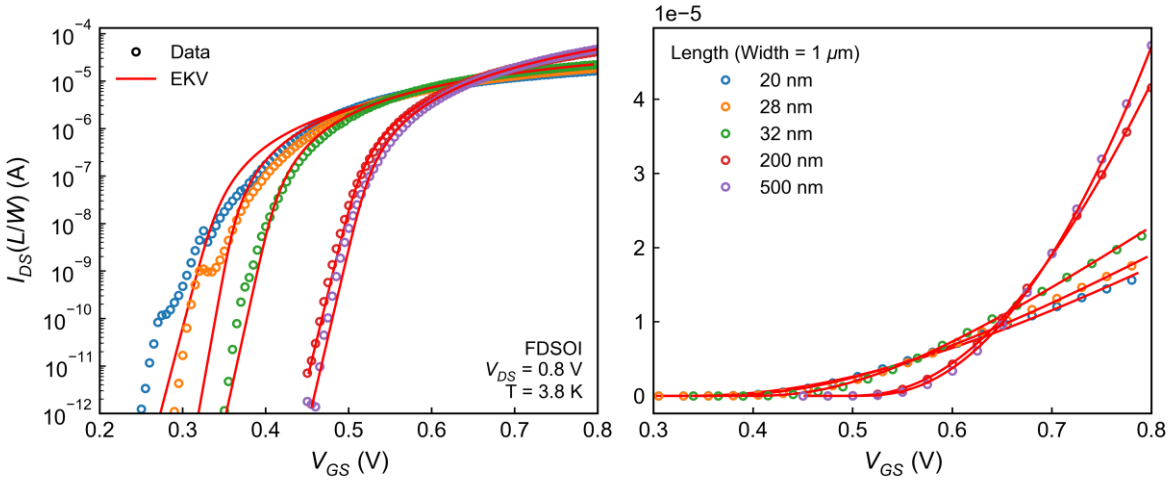


Fig. 5: sEKV model validation with various channel lengths, where nMOS transistors are fabricated by the commercial 22 nm FDSOI technology and measured at V_{DS} = 0.8 V, V_{back} = 0 V and at 3.8 K. (left) and (right) show the results in log and linear scales, respectively.

quantum confinement is not included. Hence, sEKV model results in the conventional approximation on those advanced CMOS technologies without the presence of quantum confinement.

As presented in the left plots of Fig. 3 and Fig. 4, SS reduces as the temperature drops due to the temperature dependence of thermionic currents and the extractor successfully obtains the correct value of the n factor from SS. On the other hand, the extractor captures the increased V_T and mobility at cryogenic temperatures, shown in the right plots of Fig. 3 and Fig. 4. The above results illustrate the benefits of using the developed extractor on different technologies over the temperatures.

2.2.2 Model validation with various channel lengths at cryogenic temperature

Fig. 5 presents the validation of the sEKV model on a commercial 22 nm FDSOI technology with channel length scaling from 500 nm down to 20 nm. As the length is scaled, the resonant tunneling appears in the subthreshold drain current, where carriers tunnel quantum-mechanically through the gate potential barriers via quantum dots or wells [9]. This transport mechanism results in the oscillatory drain current I_{os} (see Fig. 5 left). It should be noted that in the intrinsic channel, the dopants that diffused from the source/drain area form the ionized quantum dots, which assist the carrier tunneling [10]. Hence, the total subthreshold current consists of I_{os} and the thermionic current, which theoretically has the *SS* linearly scaled with the temperature. As a result, it raises the difficulties of defining the slope factor n, originating from thermionic current in weak inversion. Therefore, the *SS* extraction module in Fig. 1 has the flexibility to extract n from the given drain current range.

Unfortunately, the humping behavior of I_{os} is difficult be captured by the sEKV model because (i) quantum tunneling is more convenient to be described in a source-injection model rather than a charge-based one (sEKV), (ii) the location of ionized quantum dots is randomly distributed around the source/drain region [10]; therefore, it shows the high variability between devices. Although the sEKV model shows the approximated estimation on subthreshold drain current with the presence of resonant tunneling, it can still give an accurate estimation of drain current in the regime above the threshold voltage.

2.2.3 Model validation with various back-gate voltages at cryogenic temperature

This paragraph addresses the sEKV modeling of long-channel FDSOI at various back-gate voltages, V_{back}, and at deep cryogenic temperature. Controlling V_{back} allows modulating the threshold voltage

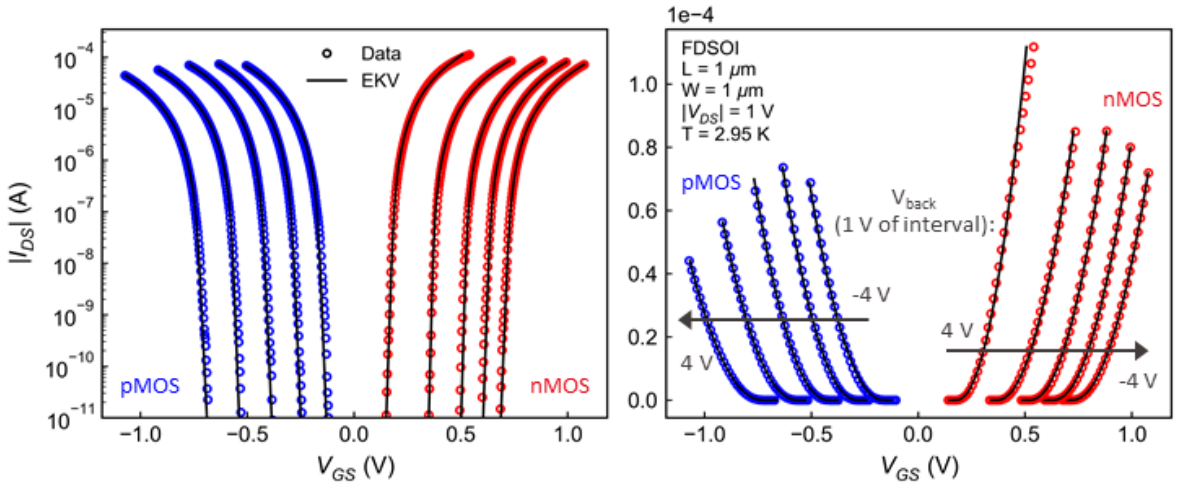


Fig. 6: sEKV model validation of nMOS and pMOS FDSOI with different back-gate voltages that transistors have W/L = 1 µm/ 1 µm and are measured at $|V_{DS}|$ = 1 V and at 2.95 K. (left) and (right) show the results in log and linear scales, respectively.

in order to compensate the increase of V_{th} at cryogenic temperatures. As shown in the right plot of Fig. 6, the forward back bias (FBB) V_{back}, which is positive for nMOS and negative for pMOS, lowers the threshold voltage. Conversely, reverse back bias (RBB) works the other way around.

Moreover, V_{back} impacts the mobility due to remote Coulomb scattering and front/back conduction separation [8] [11]. This leads to a higher mobility when a transistor is at FBB. It should be noted that the influence of V_{back} on the mobility is more pronounced at cryogenic temperatures due to the elimination of phonon-carrier interaction.

On top of that, the back-gate effects on the threshold voltage and low-field mobility μ_0 are embedded in the sEKV parameters, V_{T0} and I_{spec} ($= 2n\mu_0 C_{ox} U_T^2$), respectively. For instance, in Fig. 7, V_{T0} shows a linear dependence to V_{back}, and I_{spec}/n indicates that the highest μ_0 happens under FBB condition. Consequently, Fig. 6 shows a nice agreement of transfer characteristics between the measurement and the sEKV model at 2.95 K from deep WI to SI.

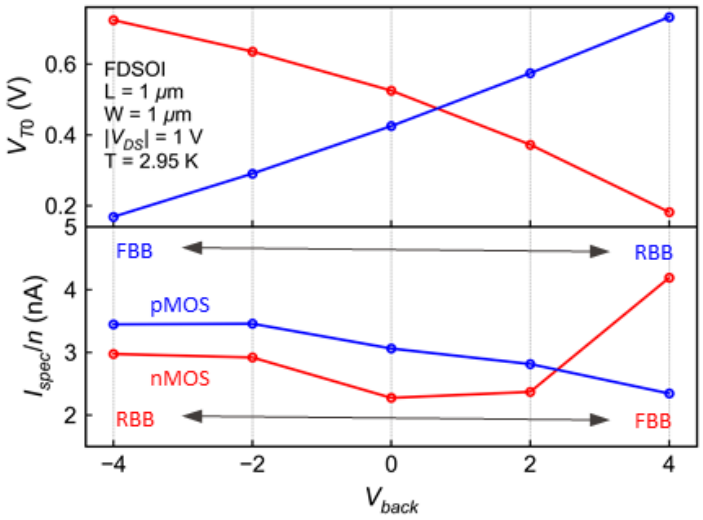


Fig. 7: sEKV parameters, which are extracted from transfer characteristics shown in Fig. 6 versus V_{back} at 2.95 K.

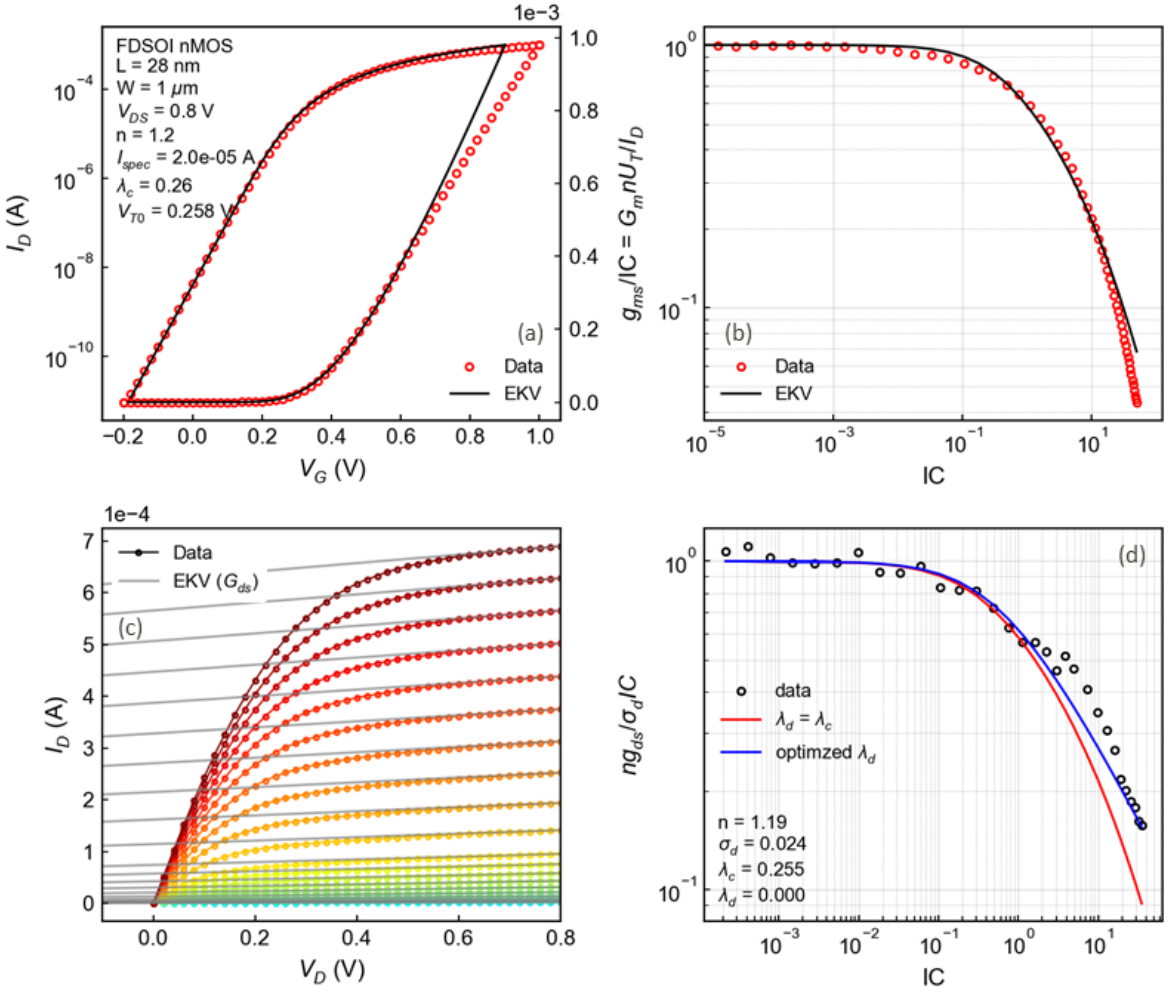


Fig. 8: sEKV model validation of transfer and output characteristics for nMOS FDSOI, with W/L = 1 µm/ 28 nm and measured at 300 K. (a) shows the measured I_D-V_G in comparison to EKV model, (b) shows the current efficiency (g_{ms}/IC) versus inversion coefficient (IC), (c) presents the I_D-V_D from weak to strong inversion, where the modeled G_{ds} is plotted for the saturation region, (d) presents the normalized output conductance (g_{ds}) versus IC.

2.2.4 Model validation with output conductance

Given a I_D-V_G and a set of I_D-V_D characteristics with different V_G from the weak inversion to the strong inversion regime, the automated sEKV extractor follows the extraction flow shown in Fig. 1 and outputs four parameters for I_D-V_G ($n, I_{spec}, V_{T0}, \lambda_c$) and two parameters for G_{ds} (λ_d, σ_d). Fig. 8 presents a comprehensive results at 300 K, comparing the measurements with the sEKV model. Fig. 8 (a,b) show the I_D-V_G and the corresponding current efficiency, where the difference between the measurements and the model in the SI regime is due to the exclusion of the vertical field-induced mobility degradation. On the other hand, G_{ds} is estimated by Eq. (3) with the extracted parameters λ_d and σ_d, and plotted with I_D-V_D in Fig. 8 (c), where I_D-V_D is shown from the moderate to the strong inversion. Similar to the current efficiency (g_{ms}/IC), g_{ds} can be normalized with respect to IC, as shown in Fig. 8 (d). Fig. 9 is similar to Fig. 8 (c) but with the normalized drain current to emphasize the results in the deep weak inversion region. Fig. 8 (d) and Fig. 9 demonstrate that the proposed model for output conductance fits the output characteristic in the region of interest for the designer over a very wide range of inversion coefficient IC.

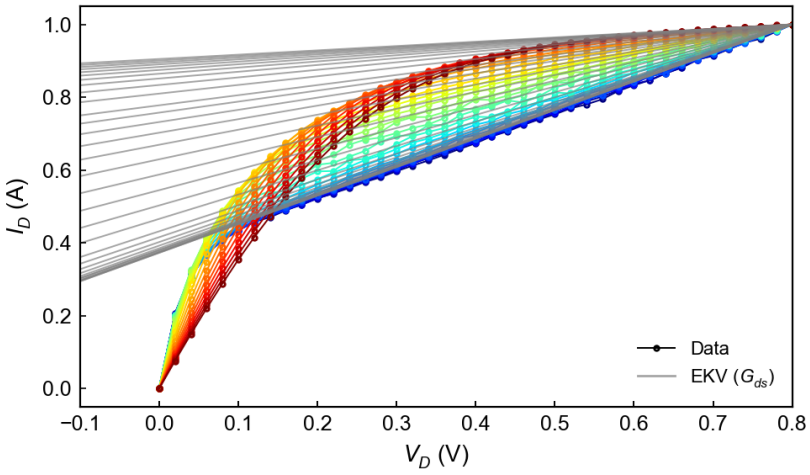


Fig. 9: Normalized drain current versus drain voltage from the WI to the SI regime, where the estimated output conductance from sEKV model is shown by the grey lines.

2.3 Cryogenic RF characterization of 22 nm FDSOI technology

This paragraph presents the cryogenic RF characterization on nMOS/pMOS DUT with a minimum channel length of a 22 nm FDSOI technology, i.e., 18 nm, from room temperature down to 3.3 K.

Fig. 10 presents the real and imaginary parts of the measured and deembedded Y-parameters at two extreme temperatures, namely 300 K and 3.3 K, for nMOS/pMOS DUT biased in SI and saturation. The capacitances, characterized by the imaginary part of the Y-parameters, do not have a significant temperature dependence. However, the increase in $\Re(Y_{21})$ and $\Re(Y_{22})$ at 3.3 K indicates the rise of G_m and G_{ds}, respectively.

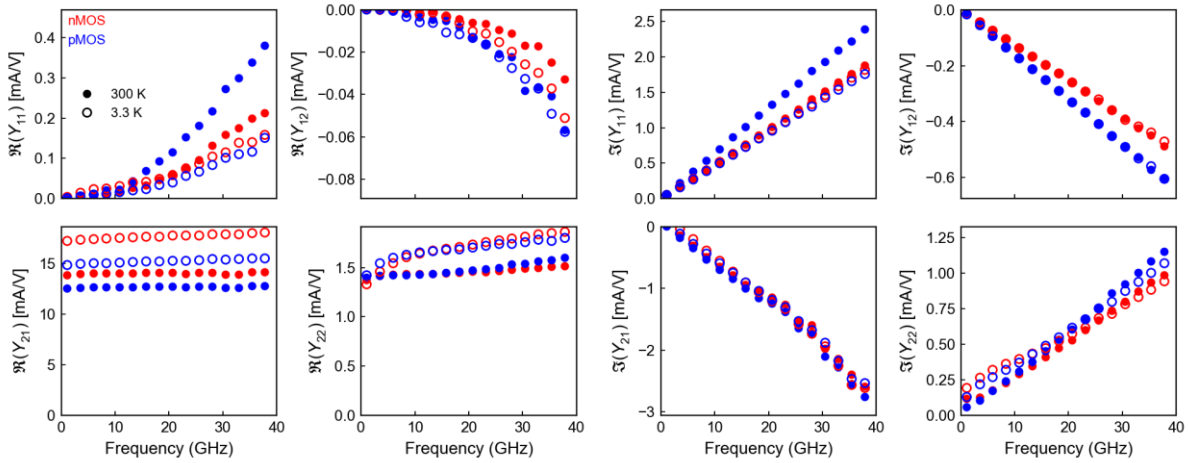


Fig. 10: Y-parameters versus frequency of RF nMOS/pMOS DUT of a 22 nm FDOSI process, with W/L = 8 µm/ 18 nm, at $|V_G| = |V_D| = 0.8\,V$, at 300 K and 3.3 K. Left four and right four show the real and imaginary parts of Y-parameters, correspondingly.

As was already observed in bulk and FDSOI technologies at room temperature and recently recognized in [11], the substrate plays an import role in RF modeling. This is clearly observed in the real part of Y_{22} shown in Fig. 10 which is affected by the nature of the substrate. The latter is modelled by a substrate network that eventually can become quite complex with numerous passive components. The more complex the substrate network, the more difficult it is to extract the related parameters which may lose their physical meaning. A particular effort will be invested into finding the simplest substrate

network which still has a physical meaning and gives reasonable results at both room and cryogenic temperatures.

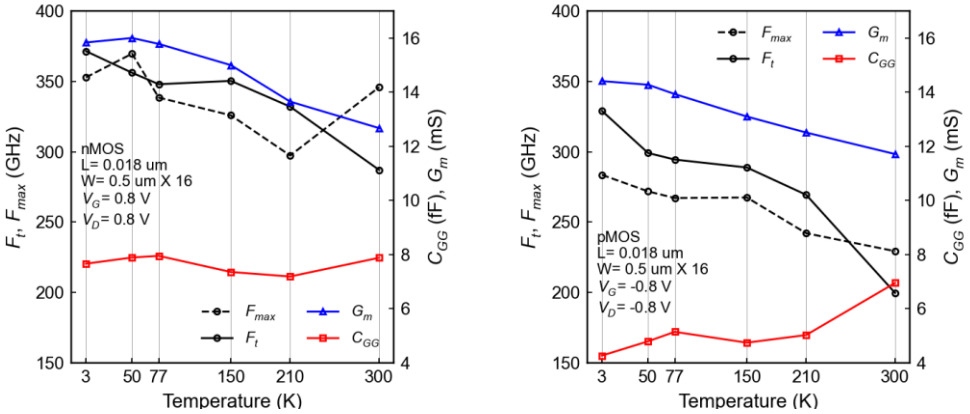


Fig. 11: FoMs versus temperature of RF nMOS/pMOS DUT of a 22 nm FDOSI process with W/L = 8 µm/ 18 nm, at $|V_G| = |V_D| = 0.8\,V$.

Some FoMs at the constant biases are plotted in Fig. 11 over a wide temperature range, including maximum oscillation frequency F_{max}, transit frequency F_t, the total gate capacitance $C_{GG} = \Im(Y_{11})/\omega$, and transconductance G_m. For nMOS, F_t and F_{max} reach to 371 and 353 GHz, correspondingly, at 3.3 K, while C_{GG} is nearly constant. On the other hand, F_t and F_{max} reach to 329 and 283 GHz, correspondingly, for pMOS at 3.3 K with a drop-off in C_{GG} from 300 to 210 K.

The RF measurments will now be used to develop a simple RF equivalent circuit and a dedicated parameter extractioin methodology that hopefully can also be fully automated. The results will be presented in details in the next Deliverable.

3 Lambert-W Function-based modelling of FDSOI MOSFETs Down to Deep Cryogenic Temperatures (INPG, LETI)

3.1 Introduction

The MOSFET electrical parameters extraction is a key topic for CMOS technology characterization and optimization. With the advent of quantum computing, requiring CMOS readout electronics at cryogenic temperatures, there is a strong need for updating MOSFET parameter extraction methodologies in advanced technologies down to very low temperatures, 4.2K and below [12], [13]. In the past years, such methodologies were developed in strong inversion region using conventional threshold voltage and mobility extraction procedures [14], [15] or specific Y-function based extraction techniques [16], [17] in bulk technologies. In addition, a full gate voltage range Lambert-W function-based methodology was recently developed allowing electrical parameters extraction in FDSOI MOSFETs at room temperature [18].

In this work, we propose, for the first time, to apply the Lambert-W function for the inversion charge and drain current modelling as a function of gate voltage and, by turn, for MOSFET parameter extraction down to deep cryogenic temperatures. To this end, we first show the validity of the Lambert-W function for the description of the gate-to-channel capacitance and inversion charge with gate voltage from weak to strong inversion in large area 28nm FDSOI MOSFETs down to liquid helium temperatures. Then, we demonstrate the applicability of the Lambert-W function-based method to fit the drain current down to very low temperatures using a classical mobility law, providing the dependence of subthreshold slope ideality factor, threshold voltage and mobility parameters with gate length and temperature.

3.2 Experiments and methods

The measurements were performed on 28nm FDSOI MOSFETs with silicon film thickness t_{si}=7nm and buried oxide (BOX) thickness t_{box}=25nm from STMicroelectronics. NMOS transistors were processed from (100) handle substrate, with <100>-oriented channel, and a high-k/metal gate Gate-First architecture [19]. Low-V_{th} transistors were available with un-doped channel through a doped back plane (NWELL doping N_A=10^{18}cm^{-3}) below the BOX. Thin gate oxide (with equivalent oxide thickness EOT=1.1nm) devices with gate length L varying from 30nm up to 10µm and with gate width W=1µm or 10µm were tested using a cryogenic probe station down to 4.2K.

The gate-to-channel capacitance $C_{gc}(V_g)$ was measured with an HP 4284 LCR meter at 1MHz frequency and 10mV AC level using the standard split C-V technique. The drain current $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region (V_d=30-50mV) with an HP4156 parameter analyzer. All the measurements were made at zero back bias. The MOSFET parameter extraction was performed on the $C_{gc}(V_g)$ and $I_d(V_g)$ characteristics using the same Lambert-W function based procedure as in [18] for room temperature. The equations and parameters used for the curve modelling are shown in Table 1. The $C_{gc}(V_g)$ and $Q_i(V_g)$ curves were fitted with Eqs. (5) and (6) with C_{ox} and *b* as fitting parameters. The $I_d(V_g)$ curves were modeled with Eqs. (8) and (9) with fitting parameters η, V_t, μ_0, θ_1 and θ_2. A conventional Levenberg-Marquardt algorithm was used for the curve fitting optimization.

$$C_{gc}(V_g,T)=\frac{bQ_i(V_g,T)C_{ox}}{C_{ox}+bQ_i(V_g,T)},\quad with\ \ b=q/(hkT) \qquad (5)$$

$$Q_i(V_g,T)=\frac{C_{ox}hkT}{q}.LW(e^{\frac{V_g-V_t}{hkT/q}}) \qquad (6)$$

$$\frac{Q_i}{C_{gc}}=\frac{1}{b}+\frac{Q_i}{C_{ox}} \qquad (7)$$

$$\mu_{eff}(Q_i)=\frac{\mu_0}{1+q_1(Q_i/C_{ox})+q_2(Q_i/C_{ox})^2},\quad with\ q_1=q_{10}+R_{sd}b \qquad (8)$$

$$I_d(V_g,T)=\frac{W}{L}\,\mu_{eff}(Q_i(V_g,T))\,Q_i(V_g,T)V_d \qquad (9)$$

Table 1. Equations and parameters used for the Lambert-w function parameter extraction. where kT/q thermal voltage, C_{ox} gate oxide capacitance, η subthreshold slope ideality factor, V_t threshold voltage, μ_0 low field mobility, θ_1 and θ_2 first order and second order mobility attenuation coefficients, R_{sd} source/drain access series resistance and $\beta=W.C_{ox}.\mu_0/L$ gain factor. In Eq (6), LW means Lambert W function.

3.3 Results and discussion

3.3.1 Capacitance and inversion charge characteristics

$C_{gc}(V_g)$ characteristics were measured on large area MOSFETs with W=L=10µm for better accuracy. The inversion charge was obtained after integration of the $C_{cg}(V_g)$ curves starting from V_g=0 as is usual in split C-V technique. Typical $C_{gc}(V_g)$ and associated $Q_i(V_g)$ characteristics are shown in Fig. 12 (a)-(b)-(c) for various temperatures from 300K down to 4.2K (sample A). Note the steeper onset of the inversion charge with the temperature lowering. As proposed in [20], [21], the plot Q_i/C_{gc} vs Q_i (Fig. 12 (d)) can be used, according to Eq. (7), to extract the gate oxide capacitance from the slope, giving here $C_{ox}\approx 2\mu F/cm^2$. Note the nice superposition of the $Q_i/C_{gc}(Q_i)$ curves for all the temperatures, revealing its relative temperature independence.

Fig. 13 (a)-(b)-(c) show the best fits of the $Q_i(V_g)$ and $C_{gc}(V_g)$ characteristics, which can be obtained with the Lambert-W function model of Eqs.(5) and (6) for temperatures varying from 300K down to 4.2K. The extracted fitting parameters for V_t and η are plotted in Fig. 13 (d), indicating a quasi-linear increase of V_t with temperature decrease and a $\approx$1/T dependence of η (not shown). The excellent agreement achieved between model and experiment emphasizes the validity of the Lambert-W function to adequately describe the capacitance and inversion charge MOSFET characteristics vs gate voltage down to deep cryogenic temperatures. This fully justifies that the Lambert-W $Q_i(V_g)$ model can further be used for the drain current transfer characteristics parameter extraction.

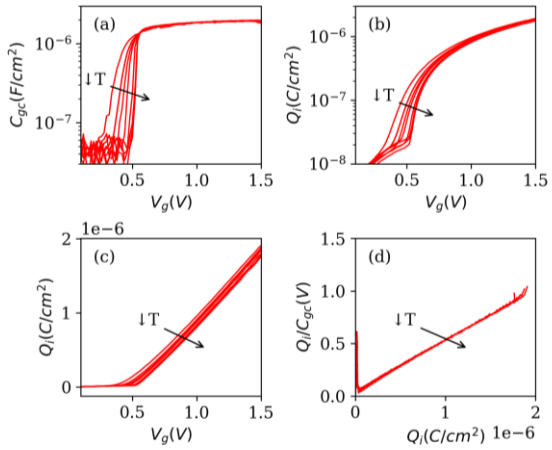


Fig. 12 $C_{gc}(V_g)$ (a), $Q_i(V_g)$ (b) and (c), and $Q_i/C_{gc}(Q_i)$ (d) characteristics for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (W=L=10µm).

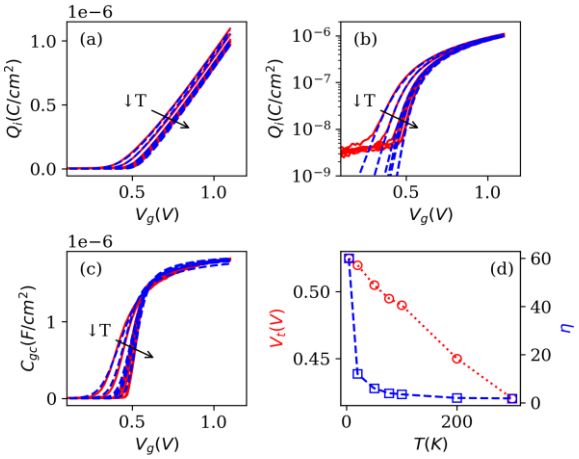


Fig. 13 Experimental (red solid lines) and Lambert-W model fitted (blue dashed lines) $Q_i(V_g)$ (a) and (b), $C_{gc}(V_g)$ (c) characteristics for various temperatures T(K)=4.2, 20, 50, 77, 100, 200 and 300 (W=L=10µm). (d) V_t and n parameter variations with temperature T.

3.3.2 Drain current transfer characteristics of long channel devices

Drain current $I_d(V_g)$ transfer characteristics were first measured in linear region (V_d=50mV) on long channel FDSOI MOSFETs with W=L=10µm to obtain the intrinsic parameters free from source/drain access resistance effect. Typical drain current $I_d(V_g)$, transconductance $g_m(V_g)$ and Y-function $Y(V_g) = I_d/\sqrt{g_m}$ characteristics are shown in Fig. 14 (red solid lines) for various temperatures from 300K down to 4.2K. Note again the strong increase of the subthreshold slope with the temperature decrease, as well as the significant increase of drain current at high gate voltage, maximum transconductance and average Y-function slope with temperature lowering. The latter features are related to the improvement of the carrier mobility as the temperature is reduced, as will be shown below.

Fig. 14 also displays the best fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), which can be reached with the Lambert-W function model of Eqs. (6), (8) and (9) for temperatures ranging from 300K down to 4.2K. The very good agreement between model and experiment underlines the usefulness of the Lambert-W function to effectively describe the drain current, the transconductance and the Y-function as a function of gate voltage from weak to strong inversion, using a classical mobility law provided by Eq. (8) down to very low temperatures.

The extracted fitting parameters V_t, η, μ_0, θ_1 and θ_2 are plotted in Fig. 14 as a function of temperature. As in the C-V extraction, the threshold voltage V_t is increasing quasi linearly with the temperature reduction, whereas the ideality factor η nearly varies as 1/T. The low field mobility μ_0 increases with temperature lowering, as is usual, due to phonon scattering reduction. The first-order mobility attenuation coefficient θ_1 lies around $\approx$-1V^{-1} over the temperature range, while the second-order attenuation coefficient θ_2 increases from 0.8V^{-2} to 1.6V^{-2} as the temperature is reduced. The latter feature is related to the higher influence of surface roughness scattering at lower temperatures. It is also worth noticing in Fig. 15 that the Lambert-W function extracted parameters V_t, η and μ_0 are close to those obtained by the Y-function method [16], emphasizing once more the consistency of the Lambert-W function method.

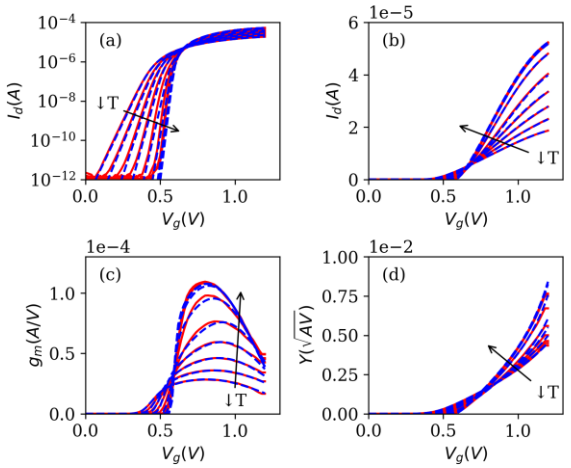


Fig. 14: Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) I_dV_g) (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (V_d=50mV, W=L=10µm).

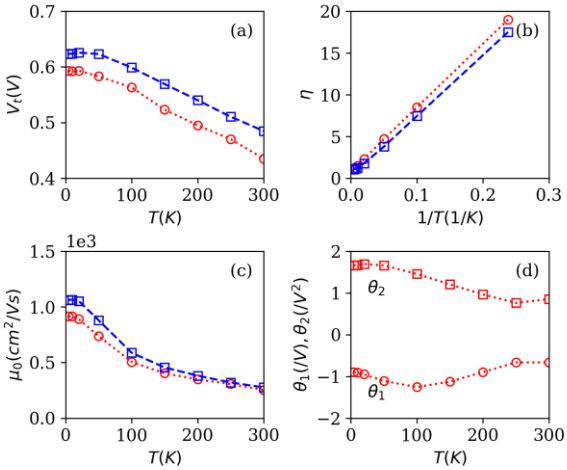


Fig. 15: V_t (a), η (b), μ_0 (c) parameter variations as extracted from Lambert-W function fits (red solid lines) and from Y-function method (blue dashed lines), and θ_1 with θ_2 (d) versus temperature (V_d=50mV, W=L=10µm).

The effective mobility μ_{eff} obtained from the Lambert-W function fits and defined in Eq.(8) has been plotted in Fig. 16(a) (red solid lines) and compared to the effective mobility determined by standard split C-V method based on $Q_i(V_g)$ data of Fig. 12 and drain current curves of Fig. 14 (blue dashed lines). As can be seen, both μ_{eff} values merge well at moderate and strong inversion, while strongly differing below threshold. The latter point can be explained, on one hand, by the finite μ_{eff} value (=μ_0) inherent to the classical mobility law used in Eq. (8) reached below threshold, and, on the other hand, by the erroneous μ_{eff} values returned by split C-V method close to and below threshold. Nevertheless, it should be noted that the maximum μ_{eff} values, μ_{max}, obtained by both methods and plotted in Fig. 16 are very close to each other, which proves the physical consistency of the mobility extracted by the Lambert-W function fits. The negative values for θ_1 obtained by Lambert-W extraction, allow modeling the increase of μ_{eff} above threshold, which is necessary for emulating the low temperature mobility law where Coulomb scattering induces such a mobility increase [17], [22].

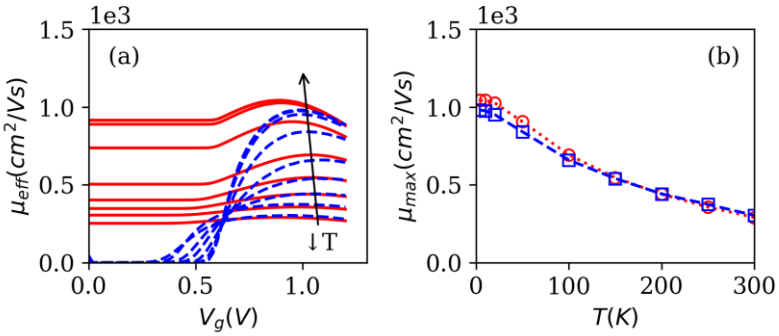


Fig. 16. (a) μ_{eff} variations with V_g and (b) maximum μ_{eff} variations with temperature as obtained from Lambert-W function fits (red solid lines) and split C-V technique (blue dashed lines). (V_d=50mV, W=L=10µm).

3.3.3 Drain current transfer characteristics of short channel devices

Drain current $I_d(V_g)$ transfer characteristics were then measured in linear region (V_d=30mV) on short channel FDSOI MOSFETs with gate length varying from 30nm up to 1µm and gate width W=1µm.

Typical drain current $I_d(V_g)$, transconductance $g_m(V_g)$ and Y-function $Y(V_g)$ characteristics are presented in Fig. 17 and Fig. 18 (red solid lines) for these various gate lengths and for T=300K and T=25K, respectively.

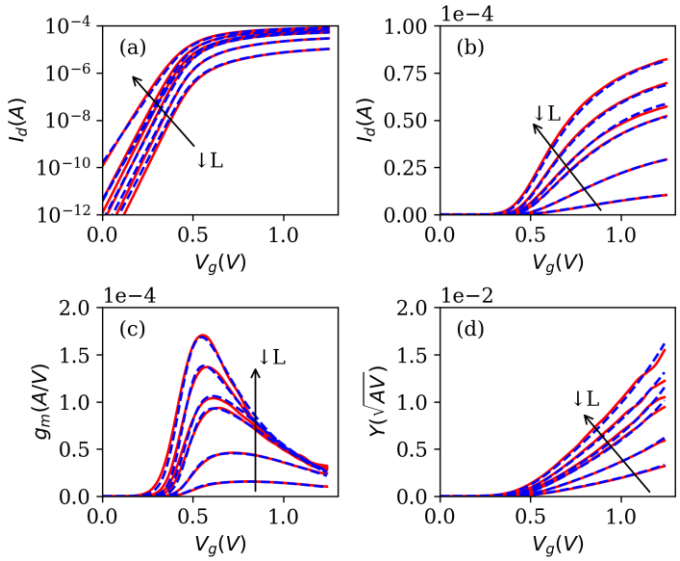


*Fig. 17: Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) I_dV_g) (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000 measured at **T=300K** (Sample C, V_d=30mV, W=1µm).*

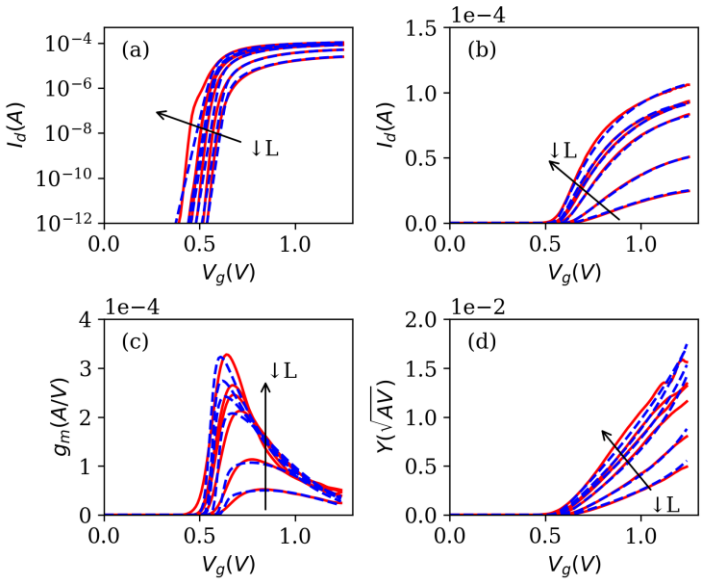


*Fig. 18: Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) I_dV_g) (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000 measured at **T=25K** (Sample C, V_d=30mV, W=1µm).*

Fig. 17 and Fig. 18 also illustrate the best fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), which can be obtained with the Lambert-W function model of Eqs. (6), (8) and (9) for the corresponding experimental data. The overall good agreement between model and experiment infers again the effectiveness of the Lambert-W function to describe the transfer characteristics, even in short channel MOS devices, as a function of gate voltage from weak to strong inversion using a classical mobility law down to very low temperatures.

The extracted fitting parameters V_t, μ_0, θ_1 and θ_2 are plotted in Fig. 19 versus gate length and for various temperatures from 25K to 300K. As can be seen, the threshold voltage V_t is exhibiting a small roll-off vs gate length due to short channel effect (SCE), whose trend is nearly independent of temperature, as expected, since being controlled only by the device electrostatics [15]. The low field mobility μ_0 displays a degradation as the gate length is reduced, more significant for lower temperatures. This mobility collapse has been previously attributed to enhanced defective scattering at small channel length, likely due to neutral point defects located near source and drain regions [23], [24]. The first order mobility attenuation coefficient θ_1 strongly increases, almost independently of temperature, as the channel length is reduced, due to the larger impact of access resistance R_{sd} in θ_1 expression (see Table 1 Eq. (8)). Instead, the second order attenuation coefficient θ_2 weakly decreases with the gate length reduction.

The extracted fitting parameters V_t, μ_0, θ_1 and θ_2 have also been plotted in Fig. 20 versus temperature for various gate lengths in order to better analyze the temperature influence. As can be seen, the threshold voltage V_t varies similarly vs T for long and short channel devices, as being governed by the same carrier statistics. In contrast, the low field mobility μ_0 variations with temperature clearly reveal a strong change in scattering mechanism signature, evolving from phonon controlled one in long channels ($\propto T^{-1}$) to neutral defect one ($\propto T^{0}$) in short channels, as already reported for advanced CMOS technologies [23], [24]. The first order mobility attenuation coefficient θ_1 is nearly constant with temperature, whereas the second order attenuation coefficient θ_2 increases with temperature lowering, similarly for all gate lengths.

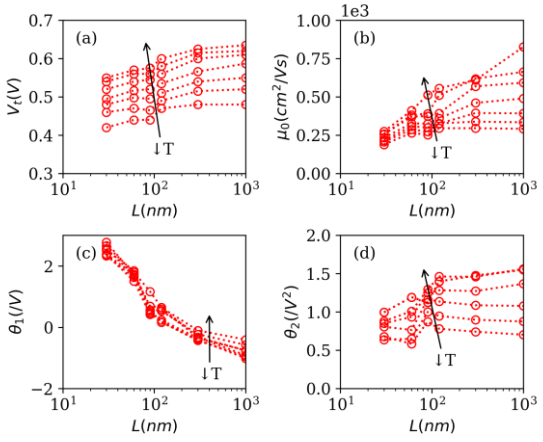


Fig. 19: V_t, μ_0, θ_1 and θ_2 parameter variations with gate length as extracted from Lambert-W function fits for various temperatures T(K)= 25, 77, 100, 150, 200, 250 and 300 (W=1µm).

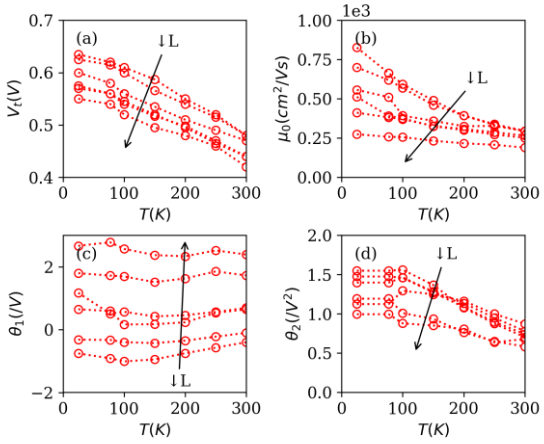


Fig. 20: V_t, μ_0, θ_1 and θ_2 parameter variations with temperatures as extracted from Lambert-W function fits for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000 (W=1µm).

Finally, Fig. 21(a) shows that the increase of the ideality factor η with the temperature reduction is similar for all gate lengths, with larger values for shorter devices due to SCE. This increase of η at lower temperature can be explained by the saturation of the subthreshold swing (SW) at temperatures below 30-40K, since $\eta=SW/(kT/q)$ [3], [2]. Fig. 21(b) displays the variations of the first order mobility attenuation coefficient θ_1 with the gain factor parameter β, parametrized by the channel lengths for various temperatures. As can be seen, θ_1 varies linearly with β as expected due to the increased influence of R_{sd} as the gate length is reduced. As is usual, the access resistance is extracted

from the slope $\theta_1(\beta)$, giving values of R_{sd} varying from 230 to 260 Ω.µm for temperatures increasing from 25K to 300K (Eq. (8)).

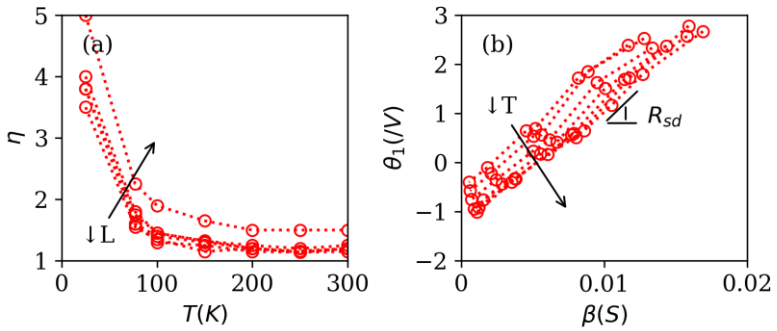


Fig. 21: (a) n parameter variations with temperature for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000. (b) θ_1 parameter variations with β=W.C_{ox}.μ_0/L gain factor for various temperatures T(K)= 25, 77, 100, 150, 200, 250 and 300 (Sample C, W=1µm).

3.3.4 Drain current transfer characteristics of long channel devices in saturation region

The Lambert-W function model of Table 1 has been extended to the saturation region by integration of the dynamic conductance g_d over drain voltage V_d, which is given by:

$$g_d(V_g,V_d,T)=\frac{W}{L}\mu_{eff}(Q_i).\frac{C_{ox}hkT}{q}.LW(e^{\frac{V_g-V_t-V_d}{hkT/q}}) \tag{10}$$

where the classical mobility law $\mu_{eff}(Q_i)$ of Eq. (8) is used. Then, the drain current is calculated from:

$$I_d(V_g,V_d,T)=\int_0^{Vd} g_d(V_g,u,T)du. \tag{11}$$

This yields after integration the analytical expression for the drain current:

$$I_d(V_g,V_d,T)=\int_0^{Vd} g_d(V_g,u,T)du. \tag{12}$$

$$I_d(V_g,V_d,T)=\frac{W}{L}.\mu_0.\frac{kT}{q}.n.\left[\begin{array}{l}\frac{1}{2}.\frac{C_{ox}}{q_2 n.kT/q}.ln\left(\frac{1+\frac{q_1}{C_{ox}}.Q_{iS}+\frac{q_2}{{C_{ox}}^2}.{Q_{iS}}^2}{1+\frac{q_1}{C_{ox}}.Q_{iD}+\frac{q_2}{{C_{ox}}^2}.{Q_{iD}}^2}\right)+\left(\frac{q_1}{q_2.n.kT/q}-2\right)'..\\ ..'\frac{{C_{ox}}^2}{\sqrt{{q_1}^2-4q_2}}.\left(atanh\left(\frac{q_1+2.\frac{q_2}{C_{ox}}.Q_{iS}}{\sqrt{{q_1}^2-4q_2}}\right)-atanh\left(\frac{q_1+2.\frac{q_2}{C_{ox}}.Q_{iD}}{\sqrt{{q_1}^2-4q_2}}\right)\right)\end{array}\right] \tag{13}$$

where Q_{iS} (resp. Q_{iD}) refers to the source (resp. drain) inversion charge.

Fig. 22 shows the fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), obtained with the Lambert-W function model of Eq. (13) for the corresponding experimental data measured in saturation (V_d=1V), while using the same parameters extracted from the linear regime fits of Fig. 14.

3.3.5 Inversion charge characteristics for various back bias

The inversion charge model of Eq. (6) has also been extended to account for the influence of the back bias Vb in FDSOI structure. To this end, the back channel inversion charge has been added to the front inversion charge with appropriate partitioning as:

$$Q_{itot}(V_g,V_b) = F\left(\frac{Q_{ifront}(V_g,V_b)}{Q_{iback}(V_g,V_b)} - 1\right).Q_{ifront}(V_g,V_b) + F\left(\frac{Q_{iback}(V_g,V_b)}{Q_{ifront}(V_g,V_b)} - 1\right).Q_{iback}(V_g,V_b) \quad (14)$$

where Φ stands for the Heaviside function. The front and back inversion charges are given by their LW

$$Q_{ifront}(V_g,V_b) = C_{ox}.\frac{kT}{q}.n.G\left(\frac{V_g-V_t+Kf.V_b}{n.kT/q}\right)\left[1-\frac{ln\left(1+G\left(\frac{V_g-V_t+Kf.V_b}{n.kT/q}\right)\right)}{2+G\left(\frac{V_g-V_t+Kf.V_b}{n.kT/q}\right)}\right] \quad (15)$$

$$Q_{iback}(V_g,V_b) = C_{fb}.\frac{kT}{q}.n.G\left(\frac{V_g-V_t+Kb.V_b}{n.kT/q}\right)\left[1-\frac{ln\left(1+G\left(\frac{V_g-V_t+Kb.V_b}{n.kT/q}\right)\right)}{2+G\left(\frac{V_g-V_t+Kb.V_b}{n.kT/q}\right)}\right] \quad (16)$$

with

$$G(x) = \ln\left[1+e^{x.(x<700)}\right].(x<700) + x.(^3700). \quad (17)$$

being a function with an ad hoc exponential truncation scheme in order to avoid overload at very low temperature. The coupling coefficient Kf and Kb are related to the capacitances:

$$Kf = \frac{C_b}{C_{ox}} \quad \text{and} \quad Kb = \frac{C_{box}}{C_{fb}}. \quad (18)$$

where C_b=C_{si}.C_{box}/(C_{box}+C_{si}) and C_{fb}=C_{si}.C_{ox}/(C_{ox}+C_{si}) with C_{si} being the silicon film capacitance and C_{box} the BOX capacitance.

Fig. 23 shows the best fits of the inversion charge characteristics Qi(Vg) (blue dashed lines) as obtained with the Lambert-W function model of Eqs (14) to (18) for experimental data (red solid lines) measured for various back biases and two temperatures. It should be noted this inversion charge model could be easily employed to extend the drain current model of Eq. (13) in order to include the back bias effects.

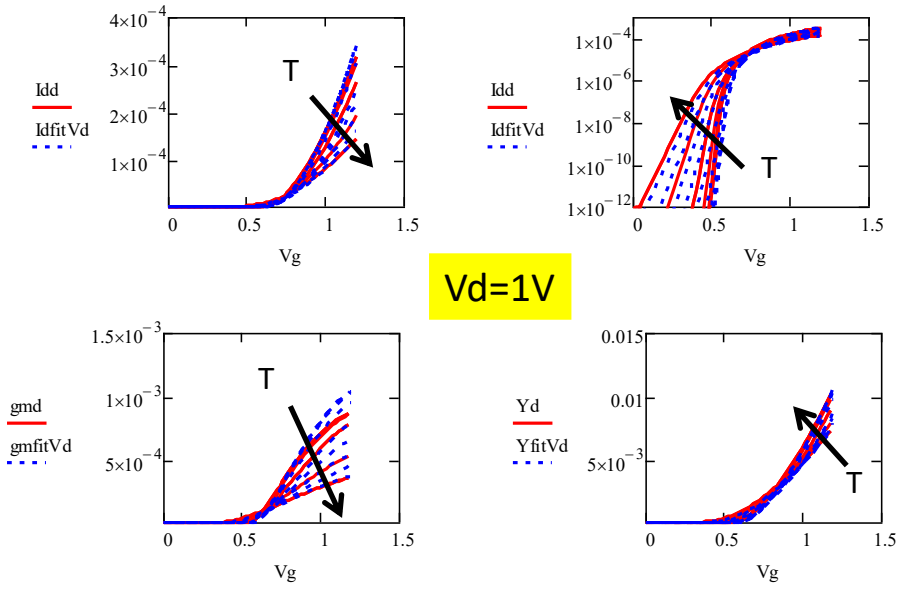


Fig. 22: Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) I_dV_g) (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 ***and 300 in saturation region*** *(**V_d=1V**, W=L=10µm).*

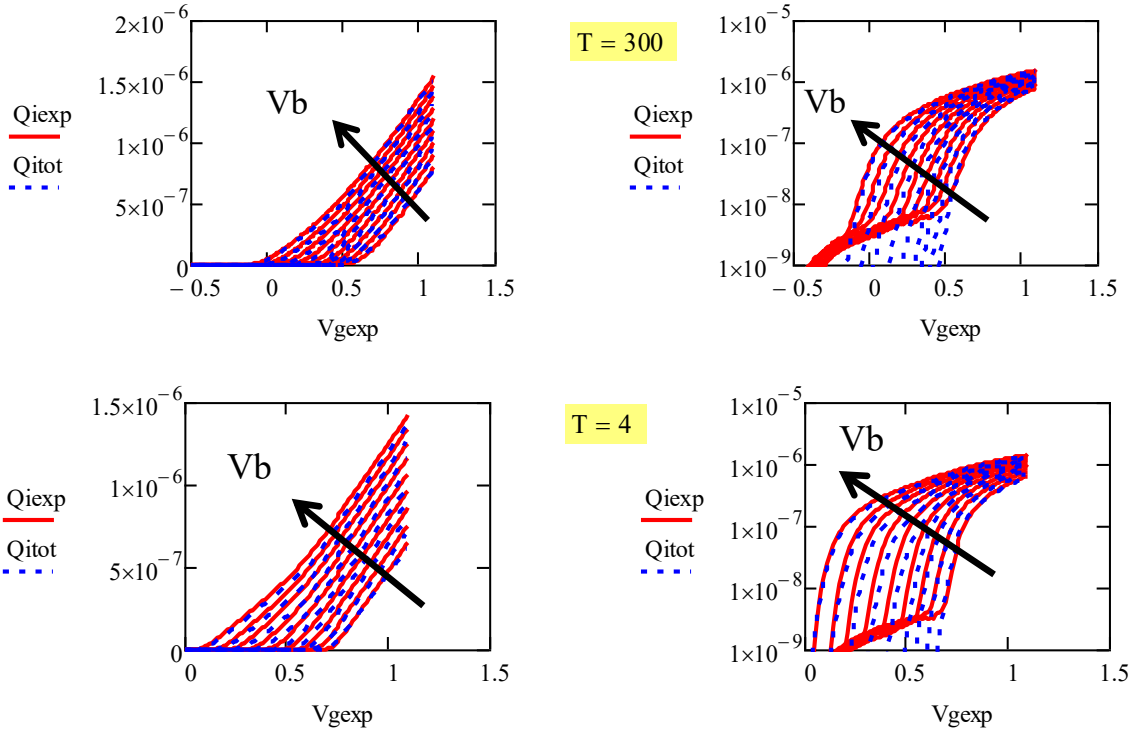


Fig. 23: Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) Qi(Vg) characteristics for various back biases Vb (V)=-3, -2, -1, 0, 1, 2, 3, 4 and 5 and for T=300K and T=4K (W=L=10µm).

4 Comprehensive Kubo-Greenwood modelling of FDSOI MOS devices down to deep cryogenic temperatures (INPG, LETI)

4.1 Introduction

The Cryogenic electronics is still a key research topic as allowing circuit performance improvements in terms of operation speed, turn-on behavior, thermal noise reduction, punch-through current decrease etc. [14], [15], [25], [26], [27]. It finds application in high speed computing, sensing and detection, space electronics and recently in readout CMOS electronics for quantum computing [12], [13]. In this context, the characterization and modelling of MOSFETs down to cryogenic temperatures is still a key issue. Besides, Kubo-Greenwood formalism has proven a powerful approach for the modelling of transport in MOS inversion layers, enabling detailed mobility calculations [22], [28], [29] and recently subthreshold slope calculations [3].

In this work, we propose to apply the Kubo-Greenwood approach for the drain current modelling as a function of gate voltage in 28nm FDSOI MOSFETs down to deep cryogenic temperatures. We first validate the single 2D subband approximation for the description of the MOS inversion charge with gate voltage down to liquid helium temperatures. Then, we show that the drain current transfer characteristics can be modeled within the Kubo-Greenwood formalism down to very low temperatures, using calibrated scattering limited mobility laws (Phonon, Coulomb, Neutral, Surface roughness).

4.2 Experiments details

The measurements were performed on 28nm FDSOI MOSFETs with silicon film thickness t_{si}=7nm and buried oxide (BOX) thickness t_{box}=25nm from STMicroelectronics. NMOS transistors were processed from (100) handle substrate, with <100>-oriented channel, and a high-k/metal gate Gate-First architecture [19]. Low-V_{th} transistors were available with un-doped channel through a doped back plane (NWELL doping N_A=10^{18}cm^{-3}) below the BOX. Thin gate oxide (with equivalent oxide thickness EOT=1.1nm) devices with gate length L varying from 30nm up to 10µm and with gate width W=1µm or 10µm were tested using a cryogenic probe station down to 4.2K.

The gate-to-channel capacitance $C_{gc}(V_g)$ was measured with an HP 4284 LCR meter at 1MHz frequency and 10mV AC level using the standard split C-V technique. The drain current $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region (V_d=30-50mV) with an HP4156 parameter analyzer. All the measurements were made at zero back bias.

4.3 Kubo-Greenwood transport and FDSOI MOSFET modelling

The main equations used for the Kubo-Greenwood transport and FDSOI MOSFET modelling are recalled in the following sub-sections.

4.3.1 Kubo-Greenwood transport modelling

The inversion layer density *n* within a single subband approximation is related to the Fermi level E_f by [22], [3],

$$n = kT.A_{2d}.ln\left(1 + e^{\frac{E_f}{kT}}\right) \tag{19}$$

where A_{2D}=g.m_d*/(π.ħ) is the 2D density of states with g the subband degeneracy factor, m_d* the DOS effective mass and ħ the reduced Planck constant and *kT* is the thermal energy, *T* being the temperature. Note that E_f is referred to the subband edge E_c, stated here to zero.

The inversion layer sheet conductivity σ, which is a function of Fermi level and temperature, can be computed by integration over energy *E* of the so-called energy conductivity function $\sigma_E(E)$ as [22], [3],

$$s(E_f, T) = \int_0^{+\infty} s_E(E)\left(-\frac{\partial f}{\partial E}\right) dE \tag{20}$$

where $f = 1/\left(1 + e^{\frac{E-E_f}{kT}}\right)$ is the Fermi function and,

$$s_E(E) = q.E.A_{2d}.\mu(E) \tag{21}$$

with *E* being the carrier kinetic energy and $\mu(E)$ the energy mobility function.

When several scattering take place in the electronic transport, the energy mobility function μ(E) can be evaluated by the Matthiessen rule as,

$$\mu(E) = \left(\frac{1}{\mu_{ph}} + \frac{1}{\mu_N} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}}\right)^{-1} \tag{22}$$

which accounts for the phonon (μ_{ph}), neutral (μ_N), Coulomb (μ_C) and surface roughness (μ_{SR}) limited mobility components, respectively.

The phonon limited mobility (in cm^2/Vs) in an inversion layer has been expressed by [30],

$$\mu_{ph}(T, F) = 1180.\left[\left(\frac{T}{300}\right)^{2.11} + \left(\frac{T}{300}\right)^{1.7}.\left(\frac{F}{F_0}\right)^{a(T)}\right]^{-1} \tag{23}$$

with *F* being the effective electric field (defined below), $a(T) = 0.2.\left(\frac{300}{T}\right)^{0.1}$ and $F_0 = 7 \times 10^4$ $(\frac{V}{cm})$ a critical field.

The Coulomb scattering limited mobility (in cm^2/Vs) is proportional to the carrier kinetic energy *E* and takes the form [22],

$$\mu_C(E) = 1650.\left(\frac{E}{E_{coul}}\right) \tag{24}$$

with here E_{coul}=0.032eV.

The surface roughness limited mobility (cm^2/Vs) is proportional to the square of the reciprocal effective electric field and is well approximated by [31]:

$$\mu_{SR}(T, F) = \frac{8.8 \times 10^{14}}{F^2}.exp\left[-\left(\frac{T}{850}\right)^2\right] \tag{25}$$

Finally, the neutral scattering limited mobility is constant with energy and temperature and reads [32],

$$\mu_N = Constant \tag{26}$$

where the constant is proportional to the reciprocal neutral defect number.

4.3.2 FDSOI MOSFET modelling

For the modelling of an FDSOI MOSFET device, we consider that the 2D inversion layer is located at the front oxide/silicon channel interface, such that the gate charge conservation equation yields,

$$V_g = V_{fb} + V_s + \frac{Q_i}{C_{ox}} + \frac{C_{it}.(V_s - V_0)}{C_{ox}} + \frac{C_b.(V_s - V_b)}{C_{ox}} \tag{27}$$

where $Q_i(E_f,T)=q.n(E_f,T)$ is the inversion charge, V_s is the front surface potential, V_{fb} is the flat band voltage, V_g is the front gate voltage, V_b is the back bias, C_{ox} the front oxide capacitance, C_{it} (=$q.N_{it}$) is the front interface trap capacitance, N_{it} being the interface trap density, and, $C_b = (C_{si}C_{box})/(C_{si}+C_{box})$ is the substrate coupling capacitance, C_{si} being the silicon capacitance and C_{box} the BOX oxide capacitance.

The surface potential $V_s(V_g,V_b)$ can be obtained by solving Eq. (27) for given front gate voltage and back bias. Thus, the Fermi level E_f can be calculated for any bias as:

$$E_f(V_g,V_b) = q.\left[V_s(V_g,V_b) - V_0\right] \tag{28}$$

where V_0 is a reference potential depending on channel doping level.

The effective electric field F entering the phonon and surface roughness limited mobility components of Eqs (23) and (25) is evaluated by the usual expression accounting for the inversion charge and back electric field as,

$$F(V_g,V_b) = \frac{\frac{Q_i(V_g,V_b,T)}{2} + C_b.\left[V_s(V_g,V_b) - V_b\right]}{\mathrm{e}_{si}} \tag{29}$$

where ε_{si} is the silicon permittivity.

The drain current is then calculated in linear operation region, i.e. for small drain voltage V_d, as,

$$I_d(V_g,V_d,V_b,T,F) = \frac{W}{L}.s\left[E_f(V_g,V_b),T,F\right].V_d \tag{30}$$

In short channel devices, the source/drain series resistance R_{sd} effect is accounted for through Ohm's law as,

$$I_d(V_g,V_d,V_b,T,F) = \frac{\frac{W}{L}.s\left[E_f(V_g,V_b),T,F\right].V_d}{1+R_{sd}.\frac{W}{L}.s\left[E_f(V_g,V_b),T,F\right]} \tag{31}$$

4.4 Results and discussion

4.4.1 Long channel devices

$C_{gc}(V_g)$ characteristics were measured on large area MOSFETs with W=L=10µm. The inversion charge was obtained after integration of the $C_{cg}(V_g)$ curves starting from V_g=0 as is usual in split C-V technique. Experimental and modeled $C_{gc}(V_g)$ and $Q_i(V_g)$ characteristics are shown in Fig. 24 for various temperatures. They clearly reveal the adequacy of the single subband approximation of Eq. (19) and of the MOSFET approach of Eq. (27) for the modelling of the gate charge control in FDSOI MOS transistors down to liquid helium temperature. The model parameters are indicated in the caption of Fig. 24.

In Fig. 25 are reported the experimental and Kubo-Greenwood modeled $I_d(V_g)$, $g_m(V_g)$ and Y-function $\mathrm{Y(V_g)} = \mathrm{I_d}/\sqrt{\mathrm{g_m}}$ [33] characteristics for such a long channel device and for various temperatures, showing very good agreement. The best Kubo-Greenwood model fits have been achieved after proper calibration of the phonon, Coulomb and Surface roughness mobility law parameters, whose values are those displayed in Eqs (23), (24) and (25). It should be mentioned that these values are close to the original ones in [22], [30], [31]. The value of μ_N, indicated in Fig. 25 caption, has been set to a large value in the case of long channel device.

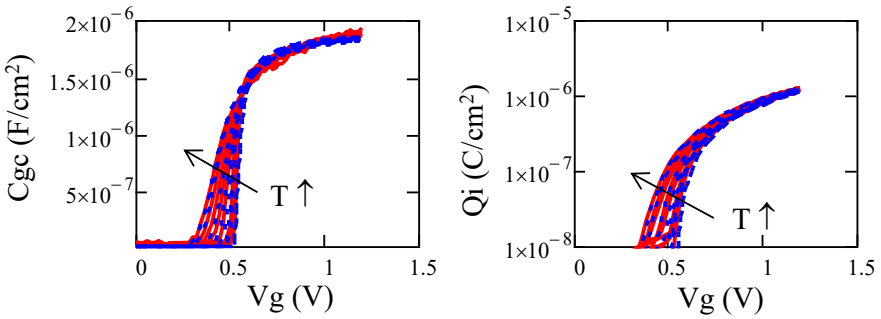


Fig. 24: Experimental (red solid lines) and modeled (blue dashed lines) $C_{gc}(V_g)$ and $Q_i(V_g)$ characteristics for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (W=L=10µm, model parameters: C_{ox}= 2.1 µF/cm², C_{box}= 0.14 µF/cm², C_{si}=1.52 µF/cm², C_{it}=0.16 µF/cm2, V_0= 0.5V).

The variations of the effective mobility, $\mu_{eff}=\sigma/(qn)$, with inversion layer density deduced from the Kubo-Greenwood modeling are shown in Fig. 26a for various temperatures. They reveal the onset of a bell-shaped mobility behavior at very low temperatures as is usual [15], [22], due to the dominance of Coulomb and surface roughness scattering processes. Figure 3b displays the change in the temperature dependence of μ_{eff} for various carrier densities taken at weak, intermediate and strong inversion.

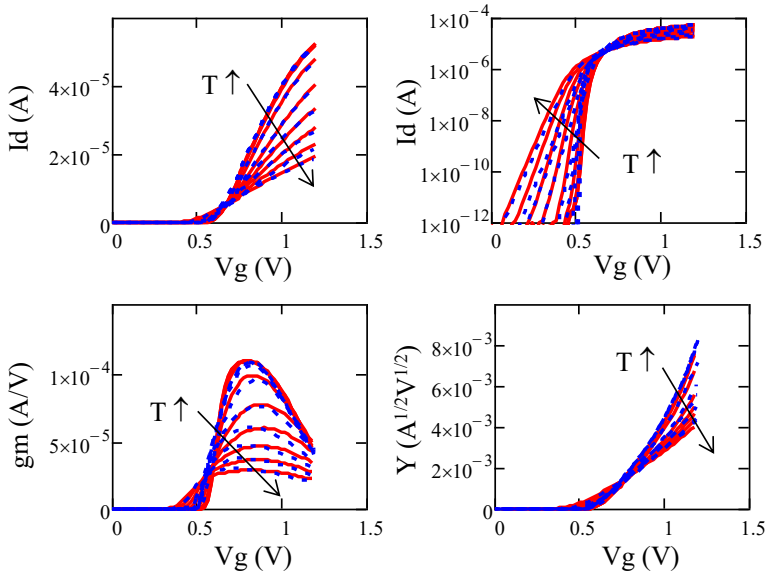


Fig. 25: Experimental (red solid lines) and modeled (blue dashed lines) I_dV_g), $g_m(V_g)$ and $Y(V_g)$ characteristics for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (μ_N=3000cm²/Vs, V_d=50mV, W=L=10µm, N_{it}=2-8×10¹²/eVcm²).

At low carrier density, μ_{eff} increases with temperature due to Coulomb scattering predominance before to decrease at higher temperature due to enhanced phonon scattering. At high carrier density, μ_{eff} always decreases with temperature due to phonon diffusion supremacy. These features are also illustrated in Fig. 27, where the variations of μ_{eff} with carrier density are compared to the various mobility law components. As expected, at very low temperature, Coulomb scattering is dominating, whereas, at high temperature, phonon scattering is prevailing.

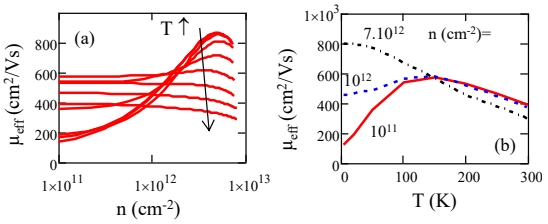


Fig. 26: a) Variations of μ_{eff} with 2D carrier density n for various temperatures T(K)=4.2, 10, 20, 50, 100, 150, 200, 250 and 300 and b) with temperature T for various 2D carrier densities as obtained from Kubo-Greenwood modeling (W=L=10µm).

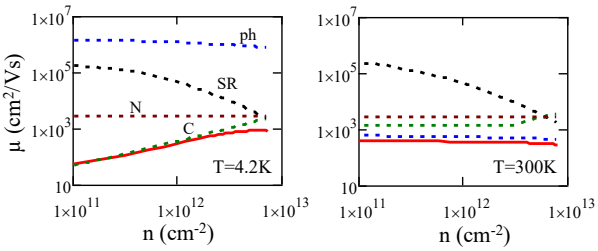


Fig. 27: Variations of μ_{eff} (red solid line) and of various scattering mobility component with 2D carrier density n for T=4.2K and T=300K as obtained from Kubo-Greenwood modeling (W=L=10µm).

4.4.2 Short channel devices

In Fig. 28 and Fig. 29 are displayed the experimental and Kubo-Greenwood-modeled $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics for MOS devices with gate length ranging from 30nm up to 1µm and for various temperature, showing again very good agreement. In this case, the best Kubo-Greenwood model fits have been obtained by keeping the same mobility parameters as for long devices (Fig. 25), at the exception of the neutral mobility component μ_N, and of the reference potential V_0, which were adjusted versus gate length for each temperature as shown in Fig. 29. It is found that V_0 follows the same trend vs L as the threshold voltage exhibiting a slight roll-off due to short channel effect (not shown). However, as can be seen from Fig. 29b, μ_N is strongly degraded as the channel length is reduced, regardless of temperature, due to the increased influence of neutral defects close to source and drain in agreement with the data of [24] (square symbols in Fig. 29b) and with the theoretical analysis of [23].

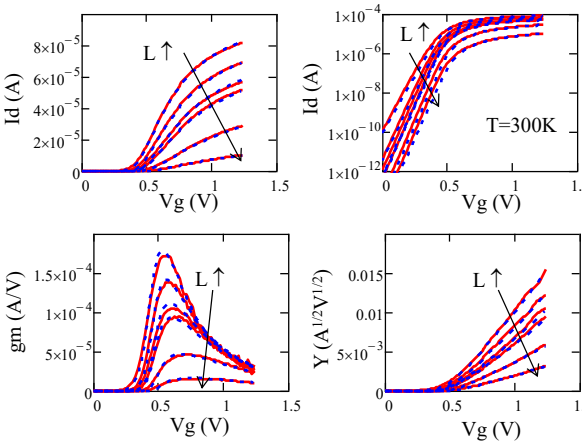


Fig. 28: Experimental (red solid lines) and modeled (blue dashed lines) I_dV_g), $g_m(V_g)$ and $Y(V_g)$ characteristics for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000 and T=300K (V_d=30mV, W=1µm).

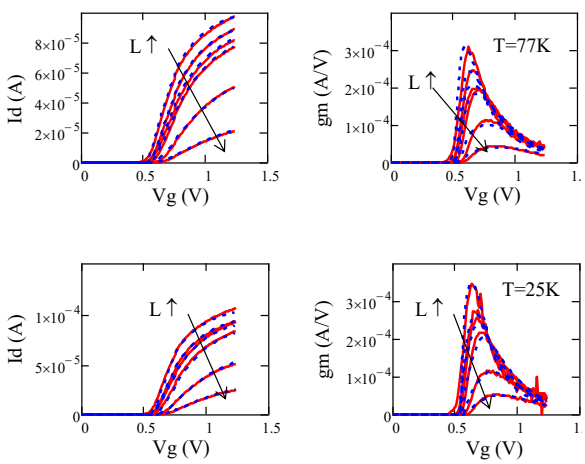


Fig. 29: Experimental (red solid lines) and modeled (blue dashed lines) I_dV_g) and $g_m(V_g)$ characteristics for various gate lengths L(nm)=30, 60, 90, 120, 300 and 1000 and for T=77K and T=25K (V_d=30mV, W=1µm).

It should also be noted that, when fitting the transfer characteristics for short channel devices, the source/drain series resistance (R_{sd}) effects were taken care using the Y-function, which is independent of R_{sd} [33]. To this end, the mobility parameter μ_N was first tuned to adjust the experimental $Y(V_g)$ curves. Then, R_{sd} was adjusted using Eq. (31) to fit the experimental $I_d(V_g)$ and $g_m(V_g)$ characteristics.

Typical values for R_{sd} were found in the range 230-250Ω.µm for temperatures varying from 25K up to 300K.

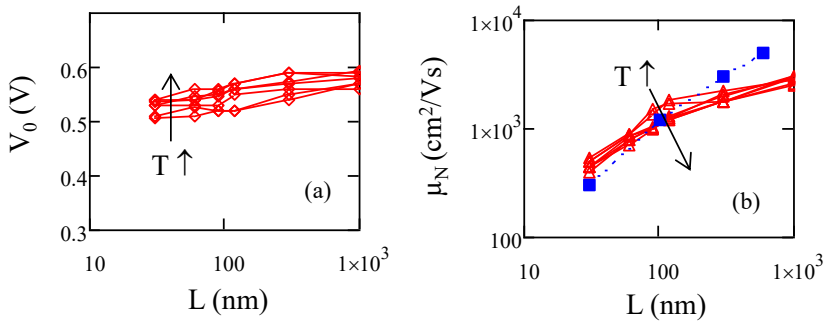


Fig. 30: Variations of (a) parameter V_0 and (b) neutral mobility component μ_N with gate length L for various temperatures T(K)= 25, 77, 100, 150, 200, 250 and 300 as obtained from Kubo-Greenwood modeling (W=1µm). The square symbols are results taken from [24].

5 Transistor models for HEMTs suitable for the design of ultra-low noise amplifiers at ambient temperatures of 300 K and 10 K (Fraunhofer IAF)

Modern circuit design relies heavily on accurate circuit simulations since they enable circuit optimizations allowing for the best performance that can be achieved. Furthermore, design cycles can be shortened, which saves time and costs. The accuracy of such circuit simulations is mainly limited by the models of the active devices. Accurate models offer the potential to achieve optimal performance for a given technology by allowing the fine tuning of circuit parameters. The extraction of cryogenic transistor small-signal models is already challenging since raising accurate measurement data is a non-trivial task. This task becomes even harder if an RF-noise model shall be extracted. Noise measurements are already challenging at room temperature and underlie a significant measurement uncertainty, which even worsens at cryogenic conditions due to unknown noise of connections into the cryostat. No off-the-shelf measurement systems are available for cryogenic noise temperature. Therefore, the extraction of temperature dependent, cryogenic noise model is extremely challenging.

In order to achieve the aforementioned benefits in cryogenic high performance circuit design, the small-signal and noise model needs to fulfill several requirements [34]. The model needs to be valid over a broad frequency range to allow the usage in arbitrary bands. Furthermore, all bias point that are usable under RF drive shall be covered by the model, which is especially important for temperature dependent noise models since the optimal noise bias point shifts to lower current and voltage bias points under cryogenic conditions. High scalability in terms of absolute gate width and gate finger numbers need to be achieved to allow for optimizations. The model needs to be valid at arbitrary ambient temperatures to allow for circuit designs dedicated to a special temperature level, which is of special importance for the integration of multiple readout functions into the cryostat as aimed by the SEQUENCE consortium.

This section reports on a scalable small-signal and noise model of a 50 nm metamorphic high-electron-mobility transistor (mHEMT) technology [35] dedicated to high performance cryogenic circuit design. The model is continuously valid down to cryogenic temperatures and up to high frequencies. All usable bias points of the modeled technology are covered by the model. In combination with the model's high scalability, the highest flexibility in RF circuit design is provided to the designer by the model.

The model uses the distributed small-signal equivalent circuit topology introduced in [36], [37]. The model is extracted for Fraunhofer IAF's new cryogenic noise optimized 50 nm mHEMT technology [38].

5.1 Temperature-Dependent Small-Signal Model

The model bases on the scalable equivalent circuit model topology described in detail in D2.2 and [36], [38].

The model is now extracted for the new 50 nm mHEMT technology, which is optimized for cryogenic ultra-low noise operation instead of the standard 50 nm mHEMT process. This mainly causes changes in the intrinsic, active part of the model, which is modeled bias and temperature dependent in addition to geometrical dependencies. Especially the intrinsic model core has a huge impact on the device noise performance. Therefore, it is important to correctly extract the intrinsic parameters and their dependencies on temperature and bias.

Each intrinsic equivalent circuit element's dependency on the temperature and the bias voltage and current is modeled by a Taylor series up to third order. Furthermore, each intrinsic parameter is linearly dependent on the gate width it describes. The intrinsic model is extracted from on-chip S-parameter measurements of single HEMTs at various temperatures and bias points via a dedicated simplex

algorithm. Fig. 31 shows the most important intrinsic parameters at different bias points as a function of temperature. The extracted model functions are compared to direct extractions from S-parameter measurements from which the extrinsic circuit has been deembedded. These S-parameters are converted to Y-parameters and conductance values are obtained from the corresponding real parts and the slope of the imaginary parts yields the capacitances.

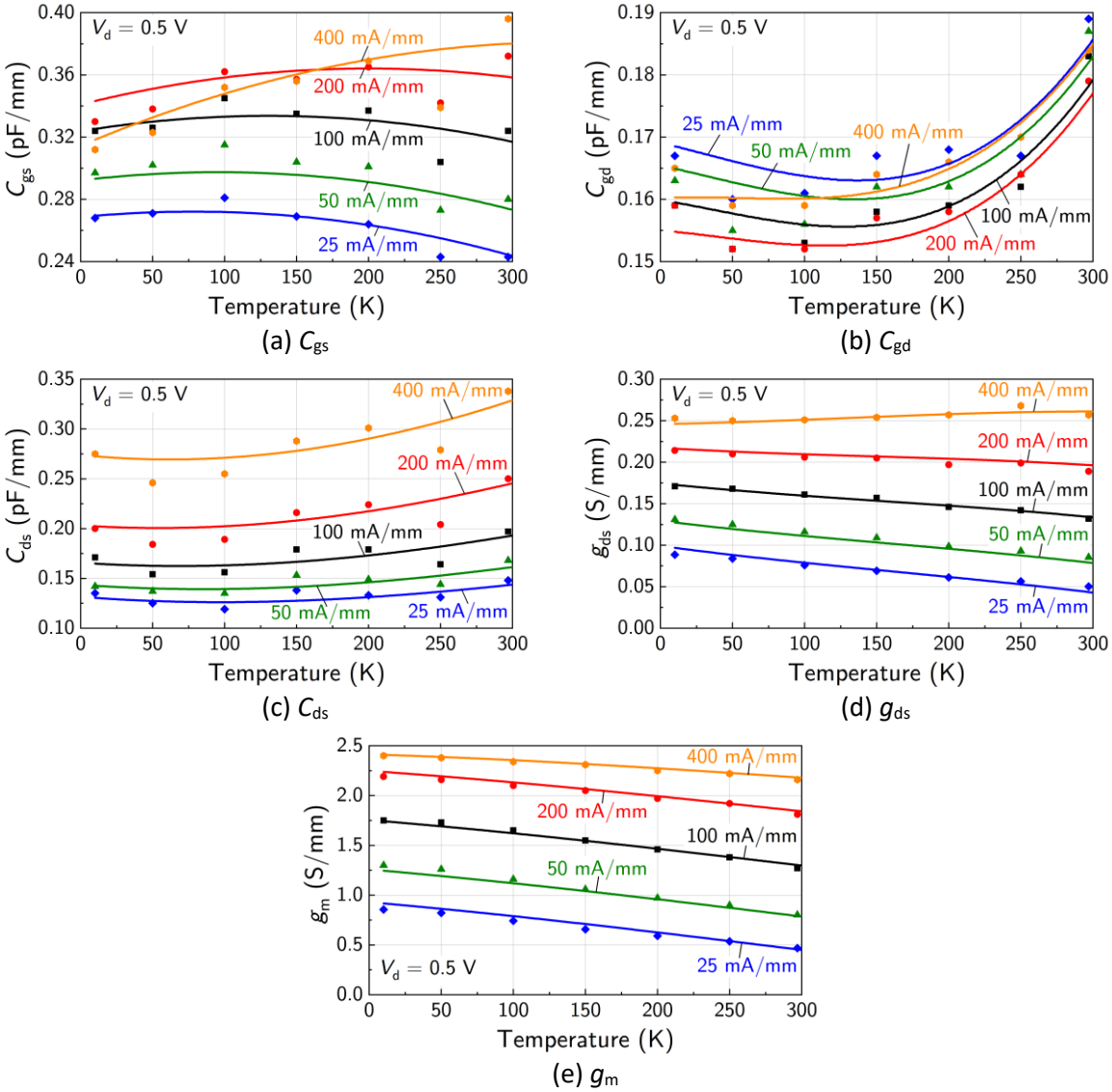
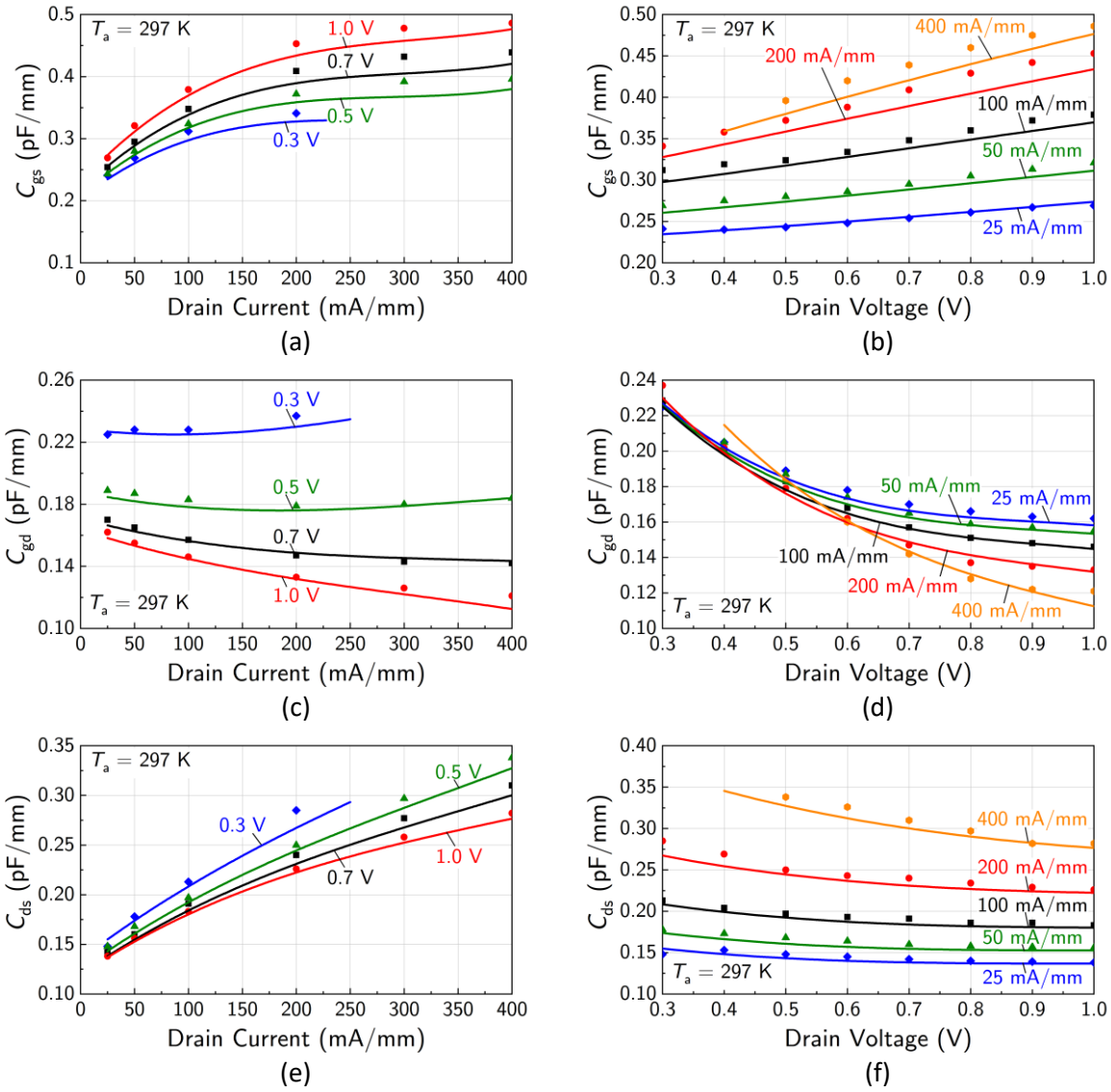


Fig. 31: Intrinsic model (lines) compared to direct extractions from S-parameter measurements (symbols) as a function of temperature. (a) C_{gs}, (b) C_{gd}, (c) C_{ds}, (d) g_{ds}, and (e) g_m are shown at various drain currents and a drain voltage of V_d = 0.5 V.

An excellent agreement between model and direct extractions is observed at various drain currents over the full temperature range considered (10 – 297 K). This indicates the validity of the approach. The intrinsic C_{gs} shows a slight increase with temperature (less than 10%) at low drain currents but is generally quite robust against temperature changes. At drain currents above 200 mA/mm, the intrinsic gate–source capacitance decreases with temperature. A qualitatively similar dependence of C_{gs} has been found in [39] for a 100-nm InP HEMT and has been motivated by the different transport mechanisms under the gate, which might cause this change of the gate–source capacitance. Both C_{gd} and C_{ds} show a slight decrease with temperature, which is likely to originate from better carrier confinement

at lower temperatures. The intrinsic g_m increases continuously when the temperature is decreased and is approximately 300 mS/mm higher at 10 K compared to the room temperature value independent of the current bias, which fits the observed dc transfer characteristics well. g_{ds} increases at lower temperatures as well, just for high drain currents above 200 mA/mm, the trend reverses and a slight decrease of g_{ds} is found.

For circuit optimizations and especially for noise modeling the dependencies of the various parameters on the bias point is important. Most applications use deep cryogenic temperatures or room temperature. Therefore, the bias dependency of the intrinsic parameters are compared to direct extractions from de-embedded S-parameters at room temperature (Fig. 32) and at 10 K (Fig. 33).



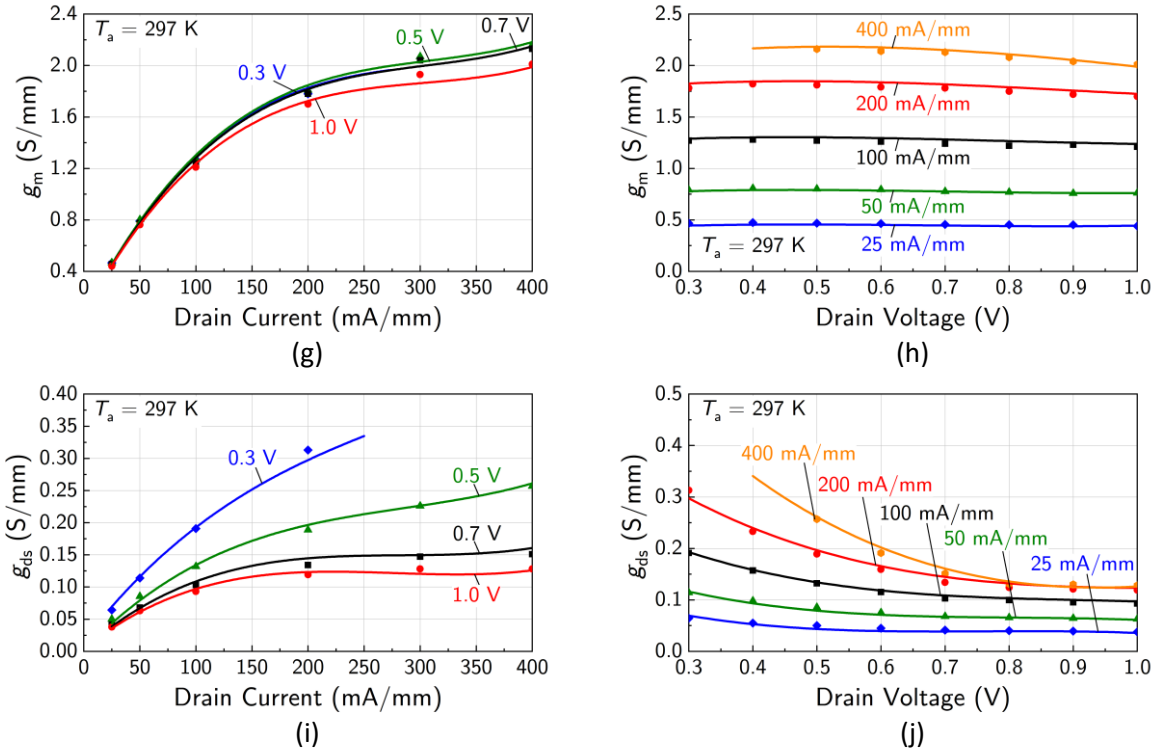
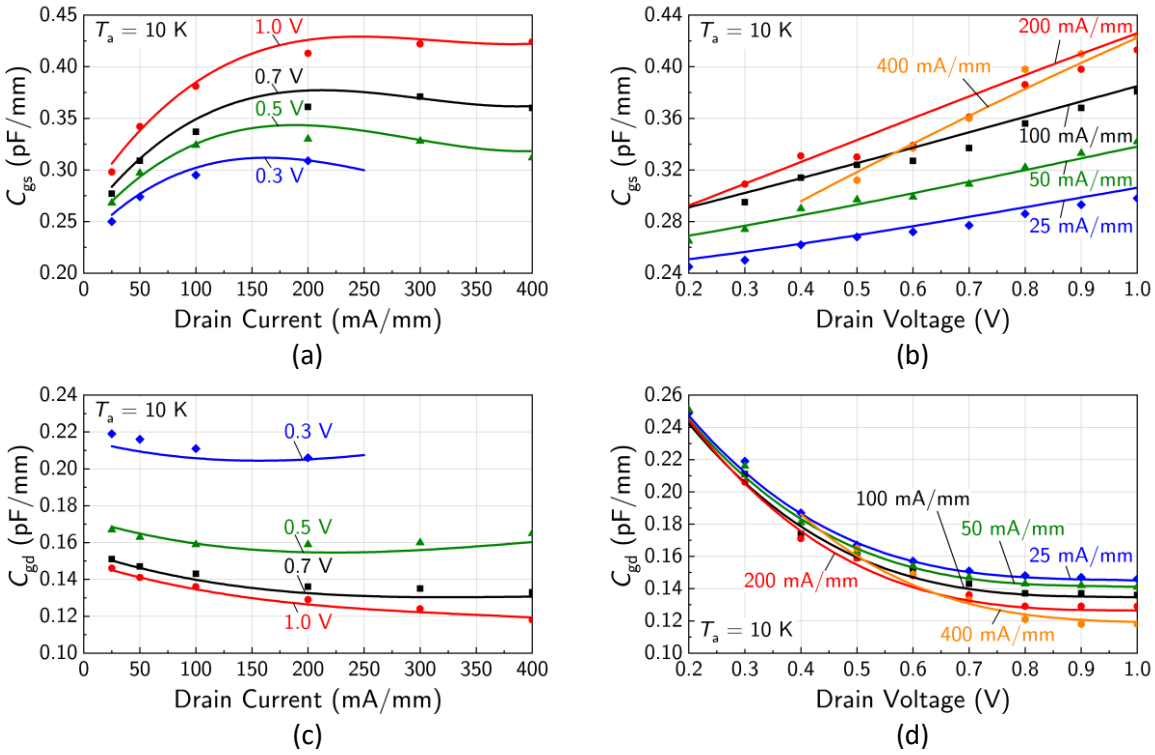


Fig. 32: Modeled intrinsic parameters (lines) and extractions from deembedded S-parameter measurements (symbols) as a function of drain current (left column) and as a function of drain voltage (right column) at T_a = 297 K. (a) C_{gs} dependent on I_d. (b) C_{gs} dependent on V_d. (c) C_{gd} dependent on I_d. (d) C_{gd} dependent on V_d. (e) C_{ds} dependent on I_d. (f) C_{ds} dependent on V_d. (g) g_m dependent on I_d. (h) g_m dependent on V_d. (i) g_{ds} dependent on I_d. (j) g_{ds} dependent on V_d are shown.



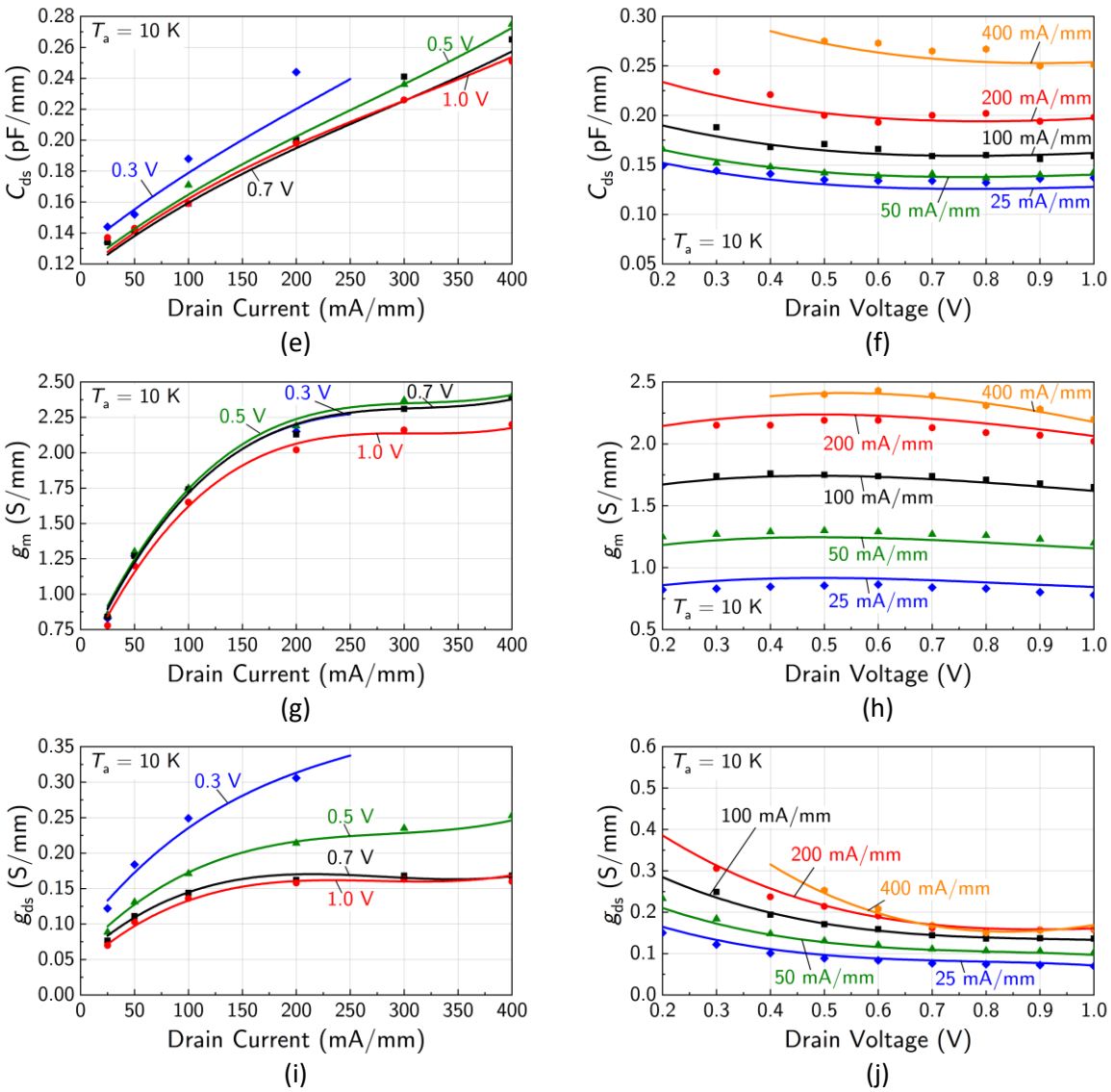


Fig. 33: Modeled intrinsic parameters (lines) and extractions from deembedded S-parameter measurements (symbols) as a function of drain current (left column) and as a function of drain voltage (right column) at T_a = 10 K. (a) C_{gs} dependent on I_d. (b) C_{gs} dependent on V_d. (c) C_{gd} dependent on I_d. (d) C_{gd} dependent on V_d. (e) C_{ds} dependent on I_d. (f) C_{ds} dependent on V_d. (g) g_m dependent on I_d. (h) g_m dependent on V_d. (i) g_{ds} dependent on I_d. (j) g_{ds} dependent on V_d are shown.

A very good agreement at both extreme temperatures is observed at all bias points. Both very low currents and voltages, as well as high voltages and currents are modeled correctly, which results in the required ability to cover arbitrary temperatures and bias points.

Regarding general trends, the intrinsic parameters show a qualitatively similar dependence on drain current and drain voltage at both temperatures. C_{gs} increases at a high rate with drain current, especially at low drain currents, but the increase settles above 200 mA/mm. At both temperatures, a linear increase of C_{gs} with drain voltage is observed. C_{gd} is quite robust against drain current changes, just at high drain voltages, a more pronounced decrease with drain current is extracted. C_{gd} decreases with increasing drain voltage as a consequence of the higher voltage applied to the gate–drain terminals. C_{ds} increases almost linearly with drain current. A slight decrease of intrinsic drain–source capacitance with increasing drain voltage is observed at high currents, but the dependence on the drain voltage is low, especially at lower currents. g_m increases at a high rate at low drain currents and the increase

flattens out above 200 mA/mm. g_m is almost independent on the drain voltage in the bias range that is considered. However, the maximum g_m is reached around 0.5 V and this maximum is more pronounced at cryogenic conditions. g_{ds} increases with drain current at a high rate at first, especially for low drain voltages, and settles at higher drain currents. g_{ds} is almost independent of the drain voltage above 0.7 V and a slight increase toward lower drain voltages is observed. This fits the typical transistor output current–voltage characteristics.

The exact extraction of the small-signal equivalent circuit parameters in all operating conditions is important to accurately determine the parameters for a temperature dependent, scalable RF-noise model. The next sub-section deals with the scalable and temperature dependent noise modeling.

5.2 Temperature-Dependent Noise Model

A noise model is included into the proposed small-signal model. The extraction relies on noise temperature measurements of LNAs at room temperature and cryogenic conditions. Room temperature S-parameter and noise measurements have been performed in one probe contact using a Keysight PNA-X vector network analyzer (VNA) with an integrated receiver and input tuner dedicated to noise measurements. This setup allows for vector corrected noise measurements using the cold-source method [40]. Cryogenic noise has been measured using the Y-factor method with a cooled attenuator [41]. The room temperature cold and hot state is provided by a Keysight 346C noise diode and the noise powers are measured on an Agilent N8975A noise figure analyzer (NFA). The attenuator is implemented as a 20 dB MMIC with integrated temperature sensor, which is wire-bonded directly to the device under test's (DUT's) input. This allows for on-chip reference plane noise measurements, which allows for precise de-embedding of passive circuit elements to obtain the noise of the active devices, namely the HEMTs. A measurement uncertainty of ±1.4 K (3σ) has been estimated for this procedure in the Ku-band.

The extraction procedure of the noise model focusses on physical parameter, which can be determined with high certainty first, before parameters that are harder to access with high certainty are extracted. Doing so allows for highest parameter accuracies. Noise can be modeled by the connection of noise generators to the equivalent circuit [42] [43] [44]. The correct determination of the magnitude of these sources is the task of the extraction.

The extrinsic part of the small-signal model describes the purely passive behavior of the transistor electrodes and their interactions. Therefore, only thermal noise at the device temperature is generated in the resistive equivalent circuit elements. The most important noise contributors of the extrinsic circuit are the gate-line resistance and the access resistances. The later ones consist of the semiconductor sheet resistance, the ohmic contact resistance, and the resistance of the ungated recess area. These resistances can be extracted via DC measurements of dedicated test structures as for example gate-line meander structures or transfer length measurements (TLM) structures via four-wire measurements. Fig. 34 shows the measured and modeled gate-line resistance, contact resistance, and semiconductor sheet resistance as a function of temperature.

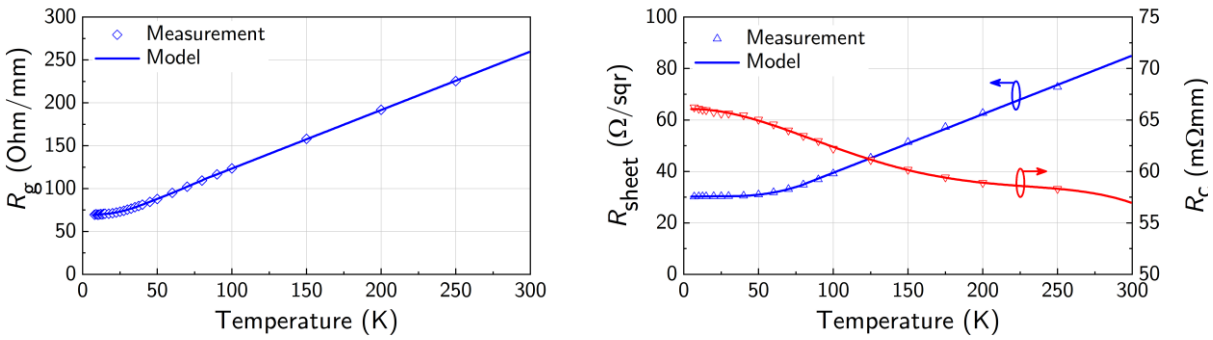


Fig. 34: Measured temperature dependence of the extrinsic resistances (symbols) and corresponding model fit (lines). (a) Gate-line resistance from a four-wire measurement of a gate-line meander structure. (b) Sheet resistance (blue triangles) and contact resistance (red flipped triangles) from four-wire TLM structure measurements are shown.

The corresponding noise voltages reduce significantly upon cooling to 10 K since the temperature decreases by approximately factor 30 and the resistance values of gate-line and sheet resistance reduce as well. Only the contact resistance shows a slight increase upon cooling, but the overall noise voltage still drops due to the enormous temperature change. The gate-line resistance is mainly determined by a 450-nm-wide metal strip of the first metallization layer that is placed on top of the T-gate. Therefore, the temperature dependence of the other electrode's resistances is modeled according to the ratio of the desired temperature to the room temperature. However, the resistance of the other electrodes is much lower compared to the extremely narrow gate electrode.

The noise caused in the active device is modeled according to a widely used HEMT noise modeling approach originally introduced by Pospieszalski [45]. Pospieszalski's approach is extended by an additional source of noise. Pospieszalksi models the noise of an intrinsic transistor with two weakly correlated noise sources: One source related to the device input, which models thermal noise of R_{gs} at ambient temperature. The other source is related to the output conductance g_{ds} and is modeled as thermal noise, but at a temperature independent of the lattice temperature. This channel noise temperature T_d exceeds the ambient temperature significantly and has been motivated to be caused by the high electrical field placed across the short gate, which accelerates the channel electrons and puts them to a higher energy. Equation (32) gives the effective channel noise current with k being Boltzmann's constant, T_d the effective channel noise temperature, g_{ds} the small-signal output conductance, and Δf the absolute bandwidth considered.

$$|\bar{\imath}_{dN}| = \sqrt{4\,k\,T_d\,g_{ds}\Delta f}. \tag{32}$$

Fig. 35 shows the equivalent circuit of the proposed intrinsic HEMT model including noise generators. Furthermore, the most important extrinsic elements causing noise are connected to the intrinsic circuit with their corresponding noise generators.

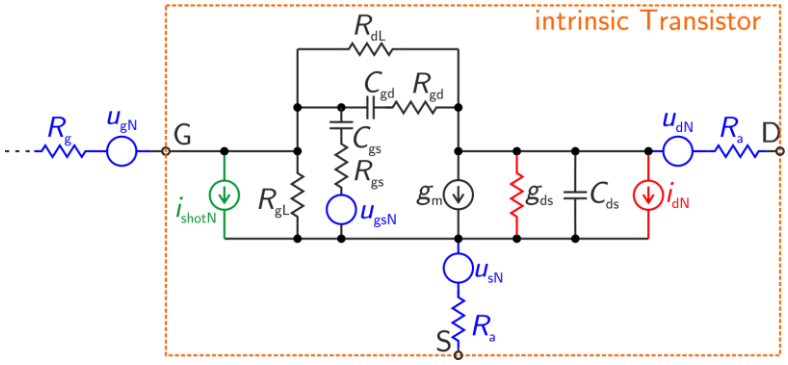


Fig. 35: Intrinsic equivalent circuit with access resistances (encapsulated by dashed line). Furthermore, a subpart of the gate-line resistance is shown. Different sources of noise are depicted by noise voltage and current generators. Blue: thermal noise at T_a. Green: shot noise due to gate current. Red: channel noise.

Pospieszalski's model is extended by an additional source of noise at the gate modeling shot noise caused by gate leakage. The magnitude of the effective shot noise current is given in (33), with the elementary electron charge q, the magnitude of the DC gate current $|I_g|$, and the absolute bandwidth considered Δf.

$$|\bar{\imath}_{shotN}| = \sqrt{2\, q\, |I_g|\, \Delta f}. \tag{33}$$

The magnitude of the effective shot noise current is directly given by the gate-leakage current, which can be determined with high certainty by DC measurements at various drain currents, drain voltages, and temperatures. The dependence of I_g on the model's input parameters (drain voltage, drain current, temperature) is modeled by a trivariate polynomial function.

The thermal noise caused by R_{gs} is modeled directly at the ambient temperature. The value of R_{gs} is quite low for the given 50-nm gate length and decreases upon cooling. Therefore, it has only a small influence of the overall device noise temperature.

Once all sources of noise that can be determined by physical means with a high certainty are determined the remaining source (the channel noise) needs to be extracted. Since a significant effort has been done in properly extracting the bias dependencies of the intrinsic parameters and especially g_{ds} the only unknown remaining is the effective channel noise temperature T_d. The extraction of T_d is done upon LNA noise temperature measurements at different temperatures and bias points.

The corresponding LNA circuit simulations are set up with the proposed HEMT model in combination with a well-established passive grounded coplanar waveguide (GCPW) library [46] in which the circuits are built. The passive library's attenuation is adapted for the cryogenic circuit simulation to correctly reproduce the reduced losses of the matching networks, which is especially important for the input matching network. The cryogenic loss of the GCPW is extracted from S-parameter measurements of a quarter wavelength resonator built of the GCPW. The channel noise temperature T_d is chosen to minimize the root-mean-square distance between noise temperature measurement and circuit simulation at various bias points. The resulting dependence of T_d at 10 K and 297 K on the drain current and the drain voltage is modeled by two bivariate Taylor series. Fig. 36 shows the modeled T_d as a function of drain current at various drain voltages (left) at 297 K and (right) at 10 K.

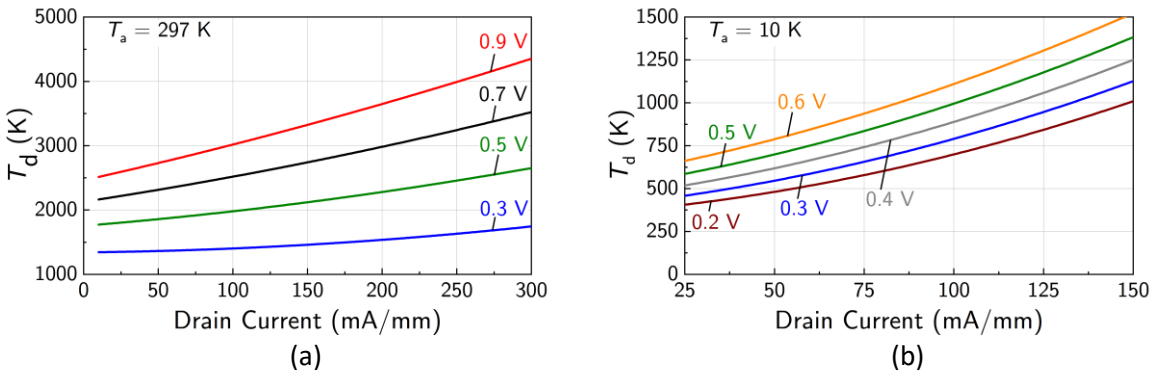


Fig. 36: Modeled channel noise temperature T_d as a function of drain current at various drain voltages. (a) 297 K and (b) 10 K are shown.

The dependence of T_d on the device temperature has been extracted from W-band LNA measurements at different temperature levels. Fig. 31 compares the extracted T_d, the corresponding g_{ds}, and the resulting effective noise current.

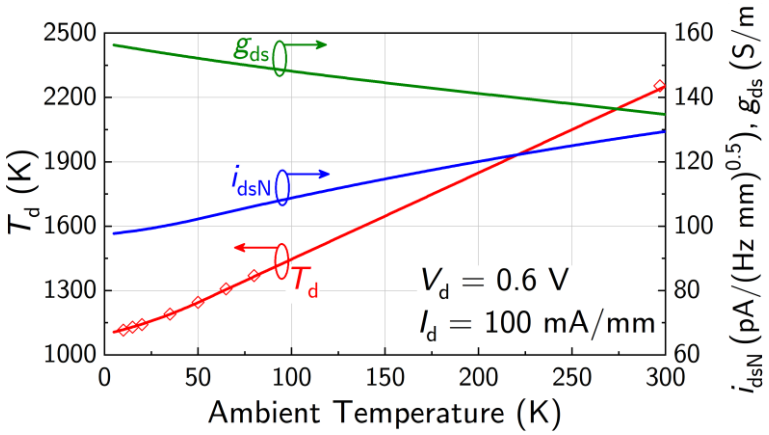
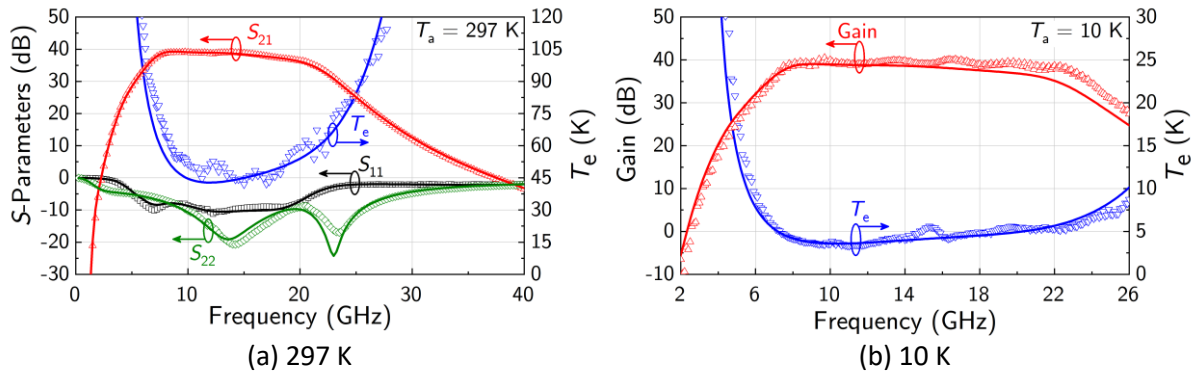


Fig. 37: Modeled channel noise temperature (red line), modeled g_{ds} (green line), and resulting magnitude of the effective channel noise current density (blue line) as a function of ambient temperature when the device is biased at V_d = 0.6 V and I_d = 100 mA/mm. Symbols depict T_d extractions from measurements.

The channel noise power approximately halves upon cooling to 10 K, however, the magnitude of the effective channel noise current only decreases by approximately 25%. This is due to the increase of g_{ds} during cooling. Given that Pospieszalski's assumption on g_{ds} modeling the physical output conductance directly holds true only a weak change in channel noise current is observed upon cooling. This fits the assumption on the high channel noise being caused by the high electrical field under the gate since the field does not change significantly upon cooling.

The proposed small-signal and noise model has been verified at both room temperature and cryogenic temperature by setting up a circuit simulation of a Ku-band LNA MMIC consisting of three 4 × 40-µm stages in 50-nm mHEMT technology with the proposed HEMT model and comparing it with S-parameter and/or noise measurements at 297 K and 10 K. This ensures that the model can be used for high performance LNA design at both room temperature and cryogenic temperature. Fig. 38 shows the circuit simulation utilizing the proposed model with corresponding measurements at 297 K and 10 K.



(a) 297 K (b) 10 K

Fig. 38: (a) On-wafer S-parameter and noise temperature measurements (symbols) of a three-stage Ku-band LNA MMIC compared to the circuit simulation utilizing the proposed mHEMT model (solid lines) at 297 K. (b) Cryogenic gain and noise temperature measurement (symbols) of the same three-stage Ku-band LNA MMIC compared to the circuit simulation utilizing the proposed mHEMT model (solid lines).

At both temperatures an excellent agreement between model and simulation is found. All resonances of S_{11} and S_{22} are correctly reproduced. Furthermore, both gain and noise temperature are correctly predicted at both temperatures. This indicates that the model is capable to be used in high performance cryogenic and room temperature circuit design.

5.3 State-of-the-Art Comparison

In this section, the proposed temperature-dependent small-signal and noise model is compared to the state of the art. A quantitative measure for the scalability of the model is needed to benchmark the scaling performance of the models. An effective measure for scalability is the ratio of the largest absolute gate width (W_g) to the lowest absolute gate width transistor that is correctly described by the model. Another useful measure is the ratio of the highest gate width finger (unit gate width, W_F) to the shortest gate width finger that is correctly modeled. The finger numbers that can be predicted are another useful measure. The combination of the three mentioned parameters is useful for a first quantitative insight into the model properties. However, no statement about the frequency regime of the model can be made from this alone. This limits the informative value of the proposed parameters on their own since it is much easier to achieve a wide scaling ratio when only low frequencies are considered. Especially, when only the lower gigahertz regime is covered by a model, it is significantly easier to obtain high scalability with a comparably simple model. This is because some parasitic effects are not as pronounced in the low-frequency S-parameters (e.g. the effect of series inductances). Therefore, it makes sense to additionally account for the absolute bandwidth in which the model is valid. A figure-of-merit (FOM) that accounts for scalability and frequency range coverage in a single number is proposed in (34). f_{max} and f_{min} are the maximal and minimal frequency that is accurately predicted by the model, respectively, and $W_{g,max}$ and $W_{g,min}$ are the maximal and minimal absolute gate width that is described by the model, respectively.

$$FOM = (f_{max} - f_{min}) \frac{W_{g,max}}{W_{g,min}}. \tag{34}$$

In Table 2, state-of-the-art scalable room temperature small-signal models published in the literature are compared to the proposed model based on the metrics aforementioned.

Table 2: State-of-the-Art Scalable Small-Signal Models at Room Temperature

Ref.	Freq. (GHz)	W_g (min. – max.) (µm)	W_F (min. – max.) (µm)	n_F (min. – max.) (a.u.)	$W_{g,max}$ / $W_{g,min}$ (a.u.)	$W_{F,max}$ / $W_{F,min}$ (a.u.)	FOM (GHz)
[47]	0.5 – 50	48 – 240	24 – 48	2 – 7	5	2	248
[47]	0.5 – 75	40 – 120	20 – 60	2	3	3	224
[48]	0.5 – 20	1000 – 4000	125 – 250	8, 16	4	2	78
[49]	0.05 – 40	64 – 96	2 – 18	4, 8, 32	1.5	9	60
[50]	0.05 – 450	10 – 120	5 – 30	2 – 4	12	6	5399
[51]	0.05 – 330	20 – 120	5 – 30	2 – 8	6	6	1980
[52]	0.25 – 110	60 – 200	15 – 100	2 – 8	3.33	6.66	366
[53]	1 – 15	120, 3600	60, 300	2, 12	30	5	420
[34]	10 – 100	180 – 200	50 – 60	4 – 6	1.11	1.2	100
[34]	2. – 48	100 – 1920	25 – 240	4 – 8	19.2	9.6	883
[34]	10 – 100	300 – 600	30 – 75	6 – 10	2	2.5	180
This Work [37]	0.1 – 150	10 – 480	5 – 100	2 – 8	48	20	7200

To the best of the authors' knowledge, the highest scaling ratio among room temperature small-signal models is achieved by the proposed model. A very wide frequency range is covered by the model as well. A few models demonstrated higher frequency range coverage, but with much narrower scalability.

Besides the room temperature performance, the temperature dependent description is compared in Table 3 using the same metrics. Only a few models demonstrated scalability at cryogenic conditions. To the best of the authors' knowledge, this is the first fully scalable model that is able to describe the small-signal and noise performance at arbitrary temperatures between 5 – 297 K.

Table 3: State-of-the-Art Temperature Dependent Small-Signal Models

Ref.	Freq. (GHz)	W_g (min. – max.) (µm)	W_F (min. – max.) (µm)	n_F (min. – max.) (a.u.)	$W_{g,max}$ / $W_{g,min}$ (a.u.)	FOM (GHz)	T_a (K)	Noise
[39]	0.2 – 50	100	50	2	1	50	5 – 350	no
[54]	0.2 – 50	80	-	-	1	50	18 – 300	yes
[55]	0.2 – 67	200	100	2	1	67	10, 300	yes
[56]	0.2 – 50	30 – 240	15 – 60	2, 4	8	200	15, 297	yes
This Work [37]	0.1 – 50	10 – 480	5 – 100	2 – 8	48	2400	5 – 297	yes

6 Temperature-dependent device modelling and compact model development for III-V nanowire MOSFETs (ULUND)

6.1 Introduction

For quantum well MOSFETs, the charge carrier density (n_s) needs to be modeled including perturbations such as band tails, nonparabolicity and interface traps in high and low density limit. The exponential band tails around the band edge with a characteristic energy (Urbach parameter) E_0 that extend inside the bandgap are demonstrated in [57]. In [1], the exponential band tails were introduced into the density of states (DOS) to explain the subthreshold swing (*SS*) saturation at cryogenic temperatures, in turn giving a good estimate of interface trap density (D_{it}) at these temperatures.

In order to include band tails, we use an empirical extension of the density of states utilizing generalized Fermi-Dirac integrals, which induce a smooth transition between the exponentially decaying DOS below the mobility edge and linearly increasing DOS above. The empirical formula of modified 2D DOS accounting for exponential band tails and nonparabolicity considering only one conduction subband is given by Eq. (35).

$$D_{2D}(E) = \frac{m_1^*}{\pi\hbar^2}\left(F_{-1}\left(\frac{E-E_1}{E_0}\right) + 2\alpha_1 E_0 F_0\left(\frac{E-E_1}{E_0}\right)\right). \tag{35}$$

The F_{-1} and F_0 are generalized Fermi-Dirac integrals of the order -1 and 0 and are given in [58]. The E_1, m_1^*, and α_1 are first subband energy level, effective mass and nonparabolicity respectively. In the limit, $E \ll E_1$, both F_{-1} and F_0 equals $e^{\left(\frac{E-E_1}{E_0}\right)}$, which reproduces the decaying DOS and for $E \gg E_1$, the standard nonparabolic DOS prevails. The fist subband energy level, E_1 differs from its equilibrium value (E_1^0) due to perturbations such as, the first order variation due to carriers present in QW and second order variation stems from the charge centroid movement towards the surface at higher V_{GS} which is obtained from Schrödinger – Poisson solver. The modified first subband energy level accounting for these effects is given in Eq.(36).

$$E_1(n_s) = E_1^0 + \frac{n_s}{C_c} - k_2 n_s^2, \text{ Where, } k_2 = 0.35H^{0.35}\ (H\ in\ nm). \tag{36}$$

The charge centroid capacitance, $C_c = \frac{\varepsilon_s\varepsilon_0}{0.397H}$ is calculated using the first perturbation theory assuming sinusoidal charge distribution in quantum well. The carrier density is calculated from the DOS and Fermi-Dirac distribution $f\left(E, E_f\right)$ given in Eq. (37). From the simple 1D electrostatics, the relation between gate voltage (V_{GS}) and surface potential (ϕ_s) is given Eq. (38). The carrier density with respect to V_{GS}, $n_s(V_{GS})$ is obtained by self-consistently solving the Eqs. (37)(38)

$$n_s(E_f) = \int_{-\infty}^{\infty} D_{2D}(E)\, f\left(E, E_f\right)\, dE. \tag{37}$$

$$(V_{GS} - \phi_s)C_{ox} = qn_s(E_f) + \int_{-\infty}^{0} D_{it}(\phi_s)\, d\phi_s. \tag{38}$$

The oxide capacitance, $C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}}$, q is the unit charge and E_f is fermi-energy level. The interface trap density is given by $D_{it}(\phi_s)$ anda gaussian trap distribution is realized here [59].

6.2 Experimental Results & Model Verification

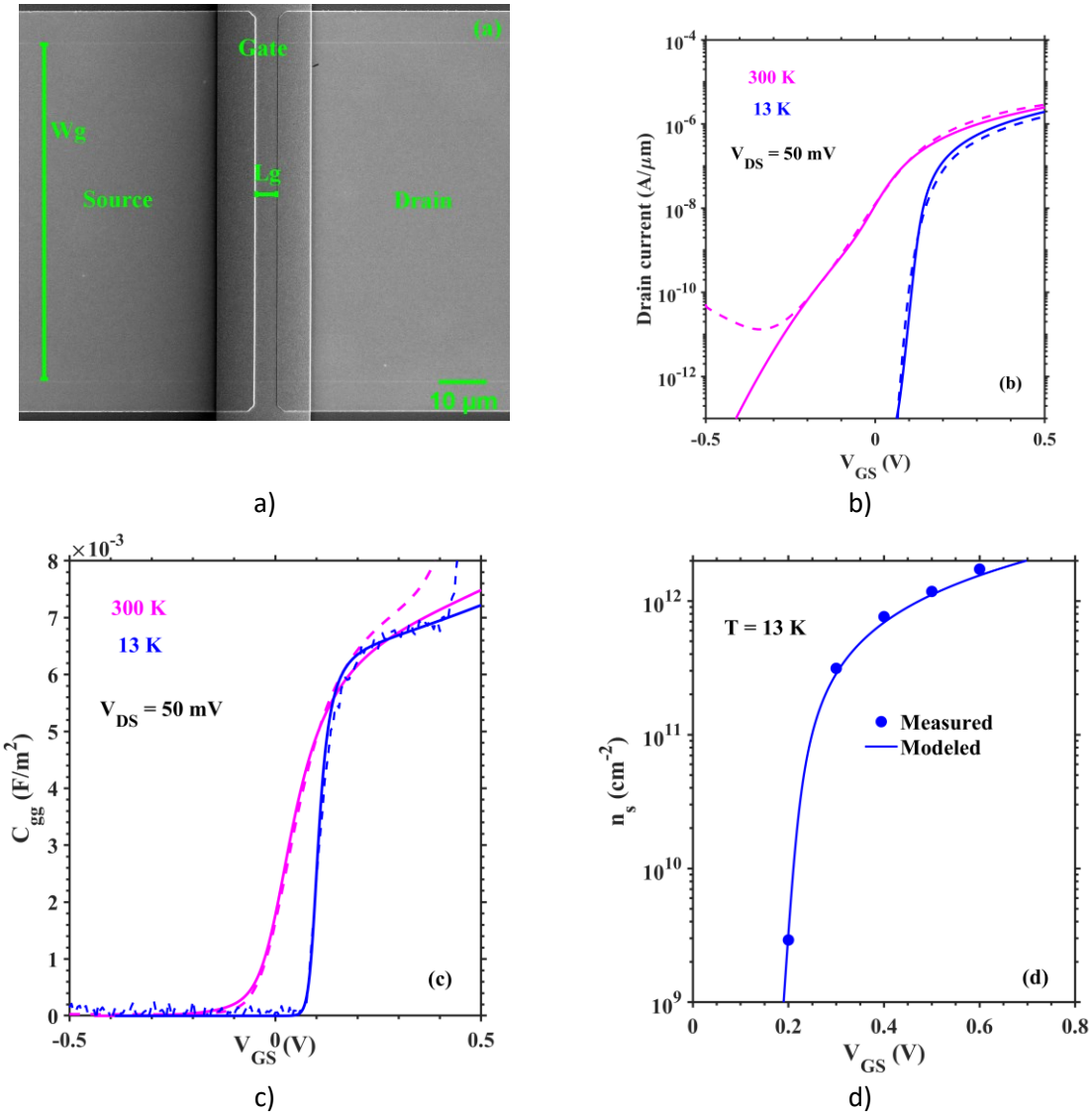


Fig. 39: (a) Top view of the fabricated long channel MOSFET with L_g = 6 µm and W_g = 70 µm, (b) Measured (dash line) and modeled (solid line) drain current vs V_{GS} (c) measured (dash line) and modeled (solid line) low frequency capacitance vs gate voltage at T = 300 K (magenta) and T=13 K (blue), (d) the measured gated hall and modeled carrier density against V_{GS}.

A 13 nm unintentionally doped and strained $In_{0.71}Ga_{0.29}As$/InP quantum well MOSFET with a gate length, L_g = 6 µm, gate width of W_g = 70 µm and Al_2O_3/HfO_2 ($\varepsilon_{ox} = 14.5, t_{ox} = 1/10\ nm$) as gate oxide are fabricated. The measurements were performed post annealing of the device at 350°C for 5 min in N_2/H_2 ambience. The SEM image of the fabricated device is shown in Fig. 39(a). The measured and modeled transfer characteristics of the device at T = 300 K & 13 K and V_{DS} = 50 mV are plotted in Fig. 39(b). In the model, the considered subband parameters are $m_1{}^* = 0.0396m_0, 0.0379m_0$ and $\alpha_1 = 1.75, 1.25\ eV^{-1}$ at T= 300 K, 13 K respectively and are calculated from 8 band k·p method. The Urbach parameter E_0, threshold voltage shift, mobility and D_{it} are the fitting parameters in the model. In a long channel MOSFET at small V_{DS}, the approximate drain current is given by $I_{DS}\left(\frac{A}{\mu m}\right) = n_s \mu(n_s)\, V_{DS}$. The QW design is similar to the sample C demonstrated in [60] and mobility is limited by charge interface scattering (CIS) and expected to be independent of temperature. The CIS is similar to remote

impurity scattering, hence $\mu \propto \sqrt{n_s}$ dependency is considered here. The $\mu(n_s) = 3.3\sqrt{n_s}$ (13 K) and $2.9\sqrt{n_s}$ (300 K), E_0 = 8 meV and a Gaussian distribution used for interface traps with $\mu_1 = 0.1\ eV, \sigma_1 = 0.15\ eV$ and N_{peak} of 1.6×10^{15} (m^{-2}eV^{-1}) at 300 K and 1.6×10^{12} (m^{-2}eV^{-1}) at 13 K are used to fit the measured data. It is noticed that the effect of interface traps is negligible at 13 K compared to RT, which can be due to multi-phonon activated interface traps. The device has SS of 78 mV/dec and 19 mV/dec at 300 K and 13 K respectively. The expected SS (13 K) with the given E_0 and D_{it} = 0 is 18 mV/dec, close to the measured value. The measured current at 300 K exhibits ambipolar nature at higher negative gate voltages.

The low frequency (1 kHz) measured and modeled C-V data at two different temperatures are plotted in Fig. 39(c). For the C-V data, the band tails mainly affect the transition between above and below threshold, as well as the sharpness of the subthreshold. At 13 K, the increase in capacitance is captured through the inclusion of second order shift in E_1 in the model. Nonparabolicity yields an increasing capacitance with V_{GS}, but for a single gate QW FET this effect is actually smaller as compared with second order shift of the subband as from Eq. (36). The sharp increase in measured capacitance in the on state is possibly due to the electron accumulation in InP under the gate pad. Gated hall measurements (B ≈ -1 T to 1 T) were performed to observe the channel carrier density variation with the applied gate voltage. The measured and modeled sheet carrier density is plotted in Fig. 39(d). The sheet carrier concentration increases with VGS and modeled data agrees with the measured data.

7 Summary and conclusions

This report presented the progress made in WP2 on the modelling of various devices at room and at cryogenic temperatures.

EFPL has reported the enhancements made on the python-based fully automatic tool for the extraction of the simplified EKV model parameters. A simple model of the output conductance is proposed that is valid from weak to strong inversion and from room temperature down to cryogenic temperature. The new output conductance model and the automatic parameter extraction tool have been validated on FDSOI 22 nm and FinFET 16 nm technologies for nMOS and pMOS and for many different geometries at various temperatures. The results demonstrate that, despite its simplicity, the simplified EKV model gives excellent fits over a large range of bias, geometries and temperatures. The effect of the backgate has been illustrated and it was shown that the I-V characteristics can be well captured by the sEKV model for various backgate voltages. Finally, the first RF measurements made on a 22 nm FDSOI at 3.3 K are presented. The next step is to develop a simple small-signal model that can capture the device behavior at RF and at cryogenic temperature including the substrate effect.

INPG/LETI has first demonstrated the applicability of the Lambert-W function-based MOSFET parameter extraction methodology on 28 nm FDSOI MOSFETs down to deep cryogenic temperatures, from long to short channel lengths. Thanks to the accurate Lambert-W function modelling of the inversion charge and drain current MOSFET characteristics from weak to strong inversion, the main parameters were extracted versus temperature and gate length, showing the temperature independence of short-channel effects and the strong mobility degradation at short channel lengths due to increased defective scattering. It should also be mentioned that this Lambert-W function modelling of the drain current has been extended to nonlinear operation region, and, therefore, could next constitute a MOSFET compact model to be used in circuit simulation at deep cryogenic conditions. INPG/LETI has also performed a comprehensive Kubo-Greenwood modelling of FDSOI MOS devices down to deep cryogenic temperatures. Interestingly, a single set of mobility parameters was only needed to fit the data versus temperature for long channel devices. Instead, in short channel MOSFETs, the neutral scattering mobility component μ_N was found to be nearly temperature independent and to significantly decrease at small gate length due to the enhanced influence of neutral defects close to source/drain ends. Therefore, such a Kubo-Greenwood modelling can provide a physical insight into the scattering processes limiting the transport in FDSOI MOSFETs down to very low temperatures and could serve as a good basis for developing compact models.

Fraunhofer IAF presented a temperature-dependent small-signal and noise model for their new cryo-noise optimized 50 nm mHEMT technology. The model is continuously scalable in terms of gate width and finger number at any temperature between 5 and 297 K. A very wide range of bias points is correctly described by the model at any temperature between 5 and 297 K. The model covers a very broad frequency range up to at least 150 GHz. This broadband performance in combination with the high model scalability set the state of the art among small-signal and noise models reported in the literature. To the best of the authors' knowledge, this is the first time that a transistor small-signal and noise model demonstrated full scalability at arbitrary temperatures between room temperature and deep cryogenic temperatures as low as 5 K. The model has been verified using measurements of a three stage Ku-band LNA MMIC at 10 K and room temperature. The corresponding circuit simulations utilizing the proposed HEMT model are in very good agreement with the measurements indicating the validity of the approach. Further verification data of the proposed model can be found in [37].

Effects due to band tails, band nonparabolicity and charge centroid movement have been implemented by ULUND for modeling of III-V narrow bandgap QW transistors, and show excellent agreement between measured and model data, and has been verified by Hall, CV and IV measurements.

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