Deliverable – D2.4

Report on extremely low temperature (20mK-4K) device characterization

Project acronym	SEQUENCE
Project number	871764
Project title	Cryogenic 3D Nanoelectronics (Sense and Readout Electronics Cryogenically Integrated for QUantum ENhanced Computation and Evolving Communication)

Document Properties	
Nature of Document	Report
Work Package	WP2 - Task 4
Task Leader	ULUND
Authors	M. Cassé, B. Cardoso-Paz (LETI), G. Ghibaudo (INPG) C. Zota (IBM)
Version	1.0
Status of Document	V1
Due Date of deliverable	M24
Actual delivery date	M26
Dissemination Level	PU

Document history			
Version	Date	Author	Status – Reason for change
0.1	2021-10-16	G. Ghibaudo	Initial Draft
0.2	2021-12-08	M.Casse, C.Zota,	First version

Release approval			
Version	Date	Name and organisation	Role
1.0	220211	Lars-Erik Wernersson	Project Coordinator

The project has received funding from the European Union's Horizon 2020 research and innovation programme under Grant agreement number 871764 (SEQUENCE)

Disclaimer:

Copyright Notice:

1 Introduction

The objectives of WP2 are i) to perform a detailed LF and RF electrical characterization and parameter extraction of the device operated under deep cryogenic conditions, and, ii) to develop associated LF and RF analytical compact device models valid at very low temperature and usable in circuit design simulation platforms. More specifically, Task 2 and Task 4 of WP2 aim at providing i) basic electrical characterization and improved parameter extraction, ii) insights into carrier transport properties (mobility, velocity) at very low temperature under degenerate statistics conditions for various devices (Si vs III-V) and iii) DC and RF electrical characterization of device operation at extremely low temperatures (20mK-4K) for physical understanding of device operation under deep cryogenic conditions for various Si and III-V devices.

The deliverable D2.4 reports on the electrical characterization carried out at extremely low temperature (20mK-4K) on 28nm Si FDSOI and FinFET devices from industrial platforms and lateral III-V devices from WP1.

2 Extremely low temperature (100mK-4K) device characterization of 28nm FDSOI MOSFETs (contributor: LETI, collaboration with INPG)

2.1 Introduction

FDSOI technology for cryogenic electronics is a very promising solution for the integrated control of qubits at ultra-low temperature [2.1]. Nearby placed MOSFET-based electronics below 1K appears necessary for the efficient operation of qubits [2.2]. Whereas good performances have been observed at temperatures decreasing down to 4.2K for various CMOS technologies, FD-SOI transistors benefit from a large V_{TH} tuning capability [2.3], [2.4]. However, no performance has been published so far at temperature as low as 100mK. Moreover, advanced FDSOI nodes have not been explored at ultra-low temperature with respect to variability [2.5], [2.6], which is essential for the development of compact models and robust design tools. Recently, two key questions have been raised concerning the application of CMOS for deep cryogenic temperatures: 1) substrate freeze-out and, therefore, back biasing efficiency in FDSOI [2.7], [2.8]; 2) dramatic increase in variability related to subthreshold current oscillations [2.6], [2.9].

In this work, variability and FDSOI performance are studied for the first time down to 100mK using extensive transistor characterization, with special focus on the two above-mentioned points. The multiplexed arrangement with an array of individually on-chip-addressed transistors to acquire statistics in a reasonable time at ultra-low temperature is particularly interesting because the readout of a large qubit array should follow a similar approach in the development of a quantum computer.

2.2 Device characteristics and setup

The measurements were performed on 28nm FD-SOI MOSFETs [2.10]. NMOS and PMOS transistors are processed from (100) handle substrate, with <100>-oriented channel and HKMG Gate-First architecture. Regular (RVT) and low (LVT) V_{TH} transistors are obtained with a doped back plane below the BOX (Fig. 2.1). Statistics and mismatch analysis were carried out down to 100mK, through an automated measuring system implemented with an on-chip multiplexed matrix arrangement of addressable transistors (Fig. 2.2). The setup was mounted on a dipstick to reach 4.2K in a liquid heli-

um bath, while measurements at 100mK were performed in a dilution fridge. Accounting for N- and PMOS, all V_{TH} flavors and W/L dimensions, ≈3000 transistors were thus characterized. The dimensions of the tested transistors range from 0.08µm to 25µm for the width W, and from 28nm up to 25µm for the gate length L. For each geometry, up to 130 pairs of identical transistors were measured at 4.2K (LT) and at RT, and up to 26 pairs at 100mK. Statistics at 100mK were not obtained at high V_{DS} to not compromise T stability during the measurements due to limited cooling power at ULT (300µW). Although all precautions were taken in order to ensure stable ambient T, one must keep in mind that due to inherent self-heating effect, a temperature rise of the device in the order of 10^6K.µm/W is expected at LT (compared to 10^5K.µm/W at RT) [2.11]. This effect severely affects MOS operation at high normalized input power (P/W) and short L.

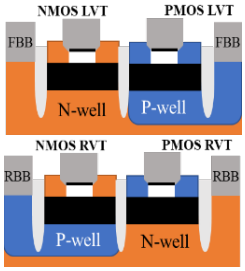


Fig.2.1. N- and PMOS 28nm FD-SOI with regular (RVT) and low-V_{TH} (LVT) flavors. t_{Si}=7nm, t_{BOX}=25nm, EOT=1.1nm, N/PWELL with typically $N_{A,D}$≈10^{18}cm^{-3}.

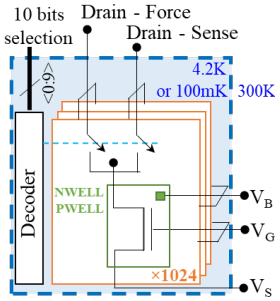


Fig.2.2. Experimental setup for variability study. Each die accounts for 512 matched pairs of transistors.

2.3 Statistics and back bias efficiency down to 100mK

Since the T decrease in the order of ≈300K leads to a significant V_{TH} increase (by typically 180mV to 250mV), forward back biasing (FBB) becomes critical in deep cryogenic applications and must be used to recover V_{TH} at LT to its value at 300K and, therefore allow power-consumption reduction and proper analog design. Fig. 2.3 shows that V_B=2V shifts V_{TH} to ≈$V_{TH,300K}$ for all studied MOSFETs in the wide range of studied dimensions (L=28nm-25µm, W=80nm-25µm). Furthermore, at LT and V_B=2V, the combined enhancement of mobility and back-interface conduction leads to I_{ON} increase, w.r.t. RT and V_B=0V (Fig. 2.4). The I_{ON} gain, calculated as the ratio of the drain current at constant gate overdrive V_{GT}=V_G-V_{TH}=0.4V for V_{DS}=0.9V measured at T=300K to the one at T=4.2K, reaches up to 5.6 times for long transistors, and reduces with L due to neutral defects and quasi-ballistic transport [2.12].

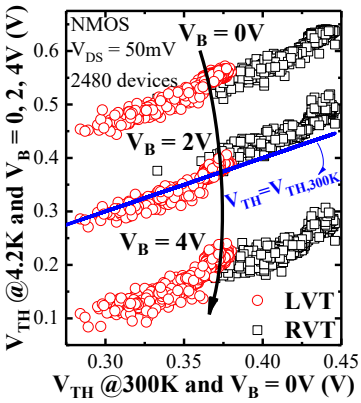


Fig. 2.3. V_{TH} at 4.2 and 300K for 2480 NMOS (all W&L tested dimensions). V_B=2V allows to compensate V_{TH} shift at 4.2K for roughly all dimensions (slope=1).

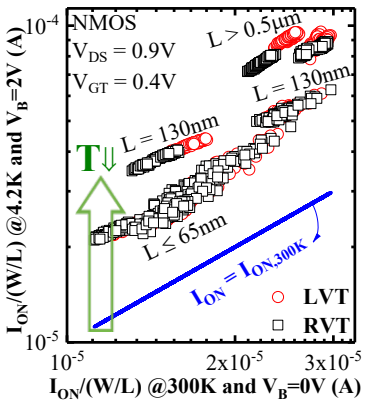


Fig. 2.4. I_{ON} at constant gate overdrive (V_{GT}=0.4V) measured at 4.2K and 300K for NMOS with several W/L. Low T and FBB (2V) highly enhance I_{ON} (up to 5.6 times, w. r. t. 300K).

A comparison of I_{DS} between 4.2K and 100mK is presented in Fig. 2.5 for all MOS devices at the same gate voltage overdrive (V_{GT}=V_{GS}–V_{TH}) for low V_{DS} and $|V_B|$=0V, 2V and 4V. The solid lines indicate that approximately the same results are obtained at 4.2K and 100mK, which agrees with the expected mobility saturation below ≈20K (i.e. no more temperature effect once phonon scattering is fully suppressed). Moreover, same V_B efficiency is kept down to 100mK for all dimensions, confirming the immunity of the doped back planes to any dopant freeze-out effect, even at ultra low temperature (Fig. 2.6). From Fig. 2.7, the superposition of the I-V characteristics at 4.2K and 100mK is also confirmed in saturation regime, upon varying V_B. The zero-T-coefficient (V_{ZTC}) [2.13] dictates the minimum V_{GS} to be applied in order to observe mobility improvement at LT. As a consequence, to get higher I_{DS} at low temperature, compared to RT, V_{GS} above ZTC or FBB is required. A larger V_{ZTC} is obtained for PMOS (Fig.8), with $|V_{ZTC}|$ above 1V, so that for PMOS, only FBB can ensure I_{DS} improvement at low T. Log scale curves in Fig. 2.8 show that SS decreases at LT (down to 8mV/K for NMOS in Fig. 2.7), which improves I_{OFF} by several orders of magnitude, well below our measurement accuracy. From the modeling point of view, it is worth noting that no additional physical effect (pertinent to FET operation) appear below 4.2K (see Figs. 2.5-2.8, where $I_{DS,100mK}$≈$I_{DS,4.2K}$), which means that compact models suitable at 4.2K can properly describe 28nm FD-SOI operation down to 100mK (and possibly **below).**

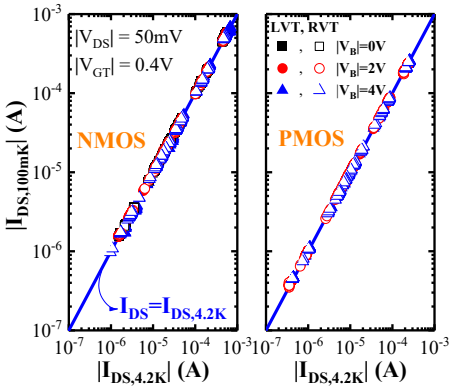


Fig.2.5. I_{DS} extracted in linear regime, at 100mK and 4.2K, for N and PMOS (all W&L dimensions). Ratio=1 is found for all transistors due to expected mobility saturation below ≈20K .

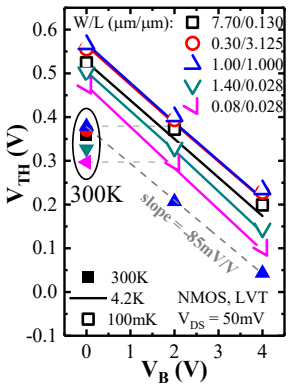


Fig. 2.6. V_{TH} vs. V_B. The NMOS body factor $\Delta V_{TH}/\Delta V_B$ is kept around -85mV/V down to 100mK.

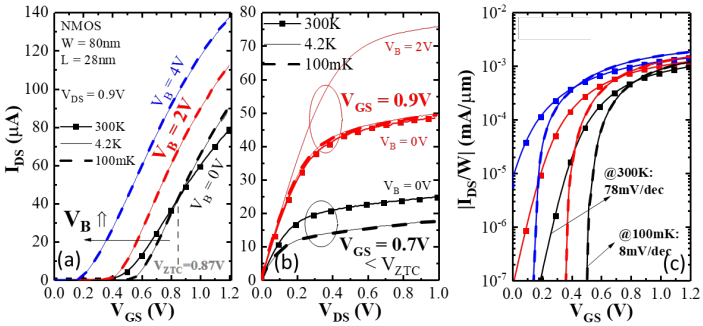


Fig. 2.7. (a) I_{DS}-V_{GS} curves in saturation in lin-scale, (b) I_{DS}-V_{DS} curves, and (c) I_{DS}-V_{GS} curves in saturation in log-scale, for temperature T= 300K, 4.2K and 100mK. I_{DS} enhancement at low T can only be obtained for V_{GS} >V_{ZTC} or FBB (w. r. t. 300K at V_B = 0V).

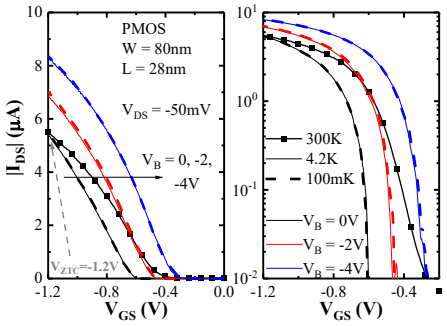


Fig.2.8. I_{DS}-V_{GS} characteristics for PMOS down to 100mK, at low V_{DS} in (left) linear scale and in (right) log scale. MOS behavior saturates below ≈20K and $I_{DS,100mK}$ ≈ $I_{DS,4.2K}$ (as also seen for NMOS in Fig. 2.7).

2.4 Subthreshold oscillations variability

The set of I-V curves in Fig. 2.9 indicate variability increase in the subthreshold regime at LT. This is related to the oscillatory current variations known to appear in short channel transistors at cryogenic T due to disorder in the channel [2.9]. According to our measurements, this phenomenon *(i)* is more pronounced as L decreases, *(ii)* is almost independent on W, and *(iii)* is stronger in PMOS (Fig.2.10). From a practical point of view, this effect can be mitigated and even supressed for L>160nm. Even though a smaller number of PMOS was measured compared to NMOS, Fig.2.10 clearly shows that PFETs are more affected with clearly observed oscillations even at high V_{DS}. Coulomb spectroscopy analysis shows "clean" Coulomb diamonds for NMOS with Single-Electron-Transistor (SET) behavior of the quantum dots having addition energies of ≈15meV, revealing that even very wide NMOS (W=1μm) could still be of interest for qubit applications (Fig. 2.11). The irregular shaped diamonds in PMOS are probably correlated to the stronger subthreshold oscillations observed in Fig. 2.10 coming from the diffusion of boron atoms from source and drain. Despite subthreshold current variability increase, this effect has no significant impact in inversion regime and only a small decrease of correlation between local fluctuations of V_{TH} in linear and saturation regime at LT (w.r.t. RT) was observed for short NMOS (Fig.2.12).

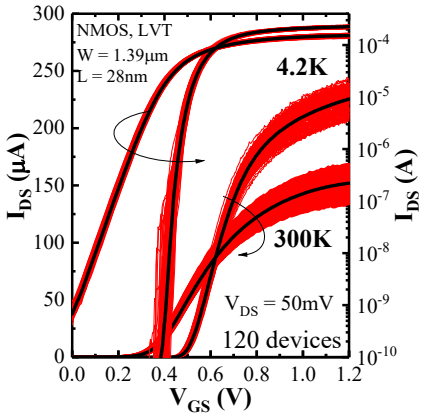


Fig. 2.9. Set of $I_{DS}(V_{GS})$ curves for 120 short NMOS at 4.2 and 300K. Bold lines indicate the mean I_{DS} values.

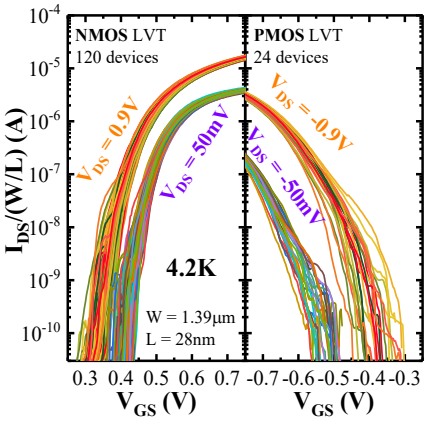


Fig. 2.10. I-V plots for N and PMOS at 4.2K. In log scale, variability is highlighted in the subthreshold regime.

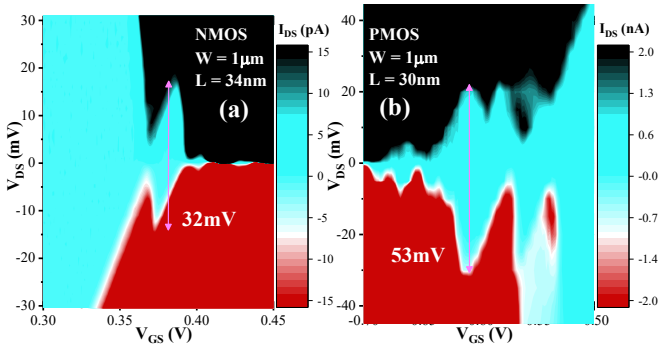


Fig. 2.11. Typical Coulomb diamonds for short N (a) and PMOS (b) showing FET-to-SET transition. PMOS exhibits disorders, leading to strong oscillations and higher subthreshold variability at low T.

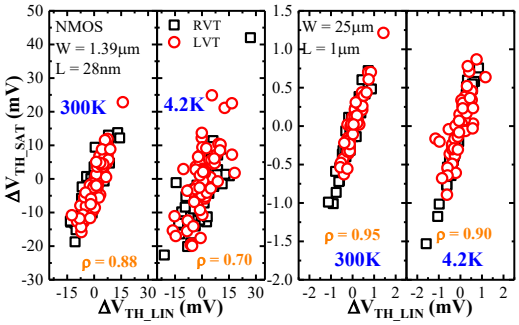


Fig. 2.12. Correlation between V_{th} mismatch (ΔV_{th}) in linear and saturation regime, at 300K and 4.2K, for a short (left) and long devices (right). Slightly degradation of correlation factor at low T due to subthreshold oscillations. Similar correlation factor at 300 and 4.2K for long MOS (no oscillation).

2.5 Threshold voltage and current variability

Fig.2.13 shows the Pelgrom plots of V_{TH} mismatch at RT and LT. $\sigma_{\Delta VT}$ follows classical Pelgrom's law at LT, like at RT, for all data points, with no specific deviation from area scaling. This reinforces that no dramatic V_{TH} variability degradation at ultra-low temperature or significant impact due to subthreshold oscillations were observed even in short PMOS, where such phenomenon proved to be more pronounced w.r.t. NMOS. At 4.2K, individual matching parameter iA_{VT} increases up to 1.60 times (w.r.t. RT) (in Fig.2.14, the error bars indicate inherent statistical uncertainty due to limited sample size), which could be attributed to the impact of band tail states [2.9], whereas metal gate granularity and charges in the gate dielectric are the main sources of V_{TH} local variability in FD-SOI [2.14].

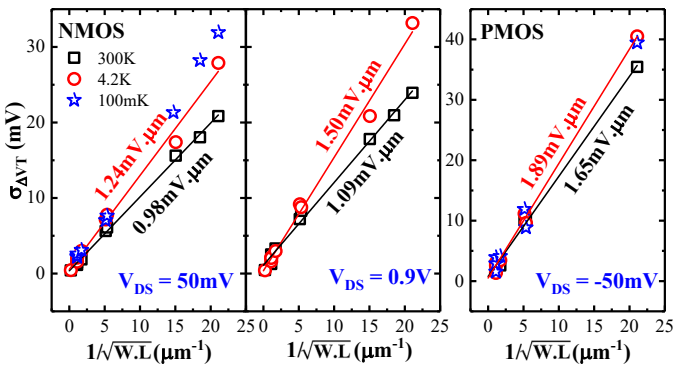


Fig. 2.13. Pelgrom plots of V_{TH} variability for NMOS (V_{DS}=50mV and 0.9V) and PMOS (V_{DS}=–50mV). Slight degradation is observed at LT.

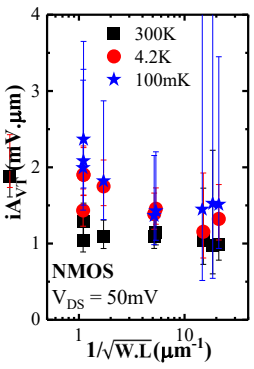


Fig.2.14. iA_{VT} vs reciprocal area square root and uncertainty limits due to finite sample size.

Current gain factor ($\beta = \mu_0.C_{OX}.V_{DS}.W/L$, where μ_0 is the low field mobility and C_{OX} is the oxide capacitance per unit area) mismatch was extracted from Y-function variability (Fig.2.15), following the procedure described in [2.15]. As expected, the increase of Coulomb/roughness scattering contribution degrades β mismatch at LT [2.16]. Fig. 2.16 shows that I_{DS} variability model Eq. (2.1) devel-

oped for room temperature, which comprises series resistance (R_S) mismatch [2.15], can still be used down to 4.2K without additional variability sources.

$$\sigma\left(\frac{\Delta I_{DS}}{I_{DS}}\right)^2 = \left(\frac{g_m}{I_{DS}}\right)^2 \sigma_{\Delta VT}^2 + (1 - g_D R_S)^2 \sigma_{\Delta\beta/\beta}^2 + g_D^2 \sigma_{\Delta Rs}^2 \quad (2.1)$$

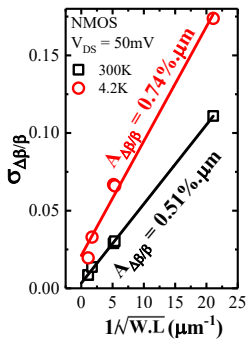


Fig. 2.15. Current gain factor variability, at RT and LT.

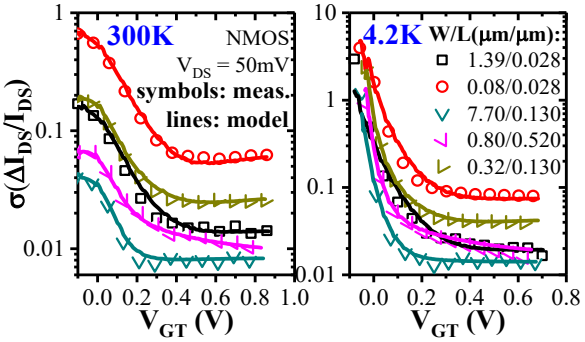
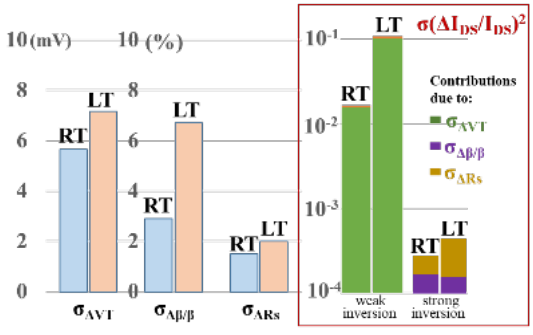


Fig. 2.16. Measurement and model $\sigma(\Delta I_{DS}/I_{DS})$. $\sigma_{\Delta Rs}$ varies from 0 to 8% of R_S = 377Ω.µm (RT) and 266Ω.µm (LT).

Fig. 2.17 summarizes the obtained variability results for each of the three main sources (V_{TH}, β and R_S) at RT and LT. At weak inversion, V_{TH} remains the main contribution for total I_{DS} variability, while β and R_S become important in strong inversion. Fig.2.18 shows that FBB can slightly improve I_{DS} mismatch in strong inversion on short devices, by pushing the inversion carriers toward the center of the Si film and thus reducing surface roughness scattering. Opposite effect is observed in long MOSFETs, which may be linked to strong intersubband scattering effect (see deliverable D2.1 and Refs.[2.17], [2.18]) when both *front* and *back* channels are activated in FBB (Fig. 2.19).



	Variability source	T dependence
$\sigma_{\Delta VT}$	Trapped charges (N_{OX}, N_{it})	↑ (+ band tail effect)
	t_{Si}, t_{OX}, t_{BOX}, workfunction, W, L	No T dependent
$\sigma_{\Delta\beta/\beta}$	Mobility: Phonon	↓ (totally suppressed)
	Coulomb (N_{OX}, N_{it})	↑ (+ band tail effect)
	Surface Roughness	No T dependent
	W, L, t_{OX}	No T dependent
$\sigma_{\Delta Rs}$	Implantation process	No T dependent

Fig. 2.17. Summary of variability contributions and T dependence for NMOS. W=1.39µm, L=28nm.

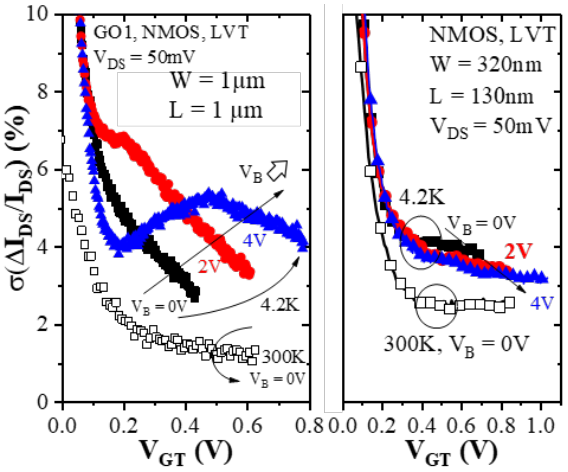


Fig. 2.18. $\sigma(\Delta I_{DS}/I_{DS})$ vs. V_{GT} varying V_B for (left) long, and (right) short devices. FBB slightly reduces I_{DS} variability on short devices, especially for high V_{GT}.

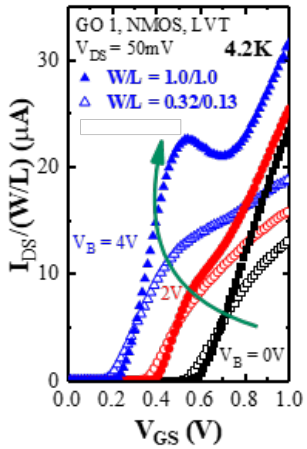
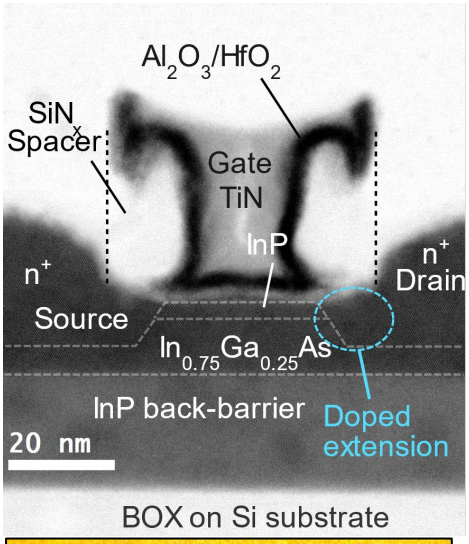
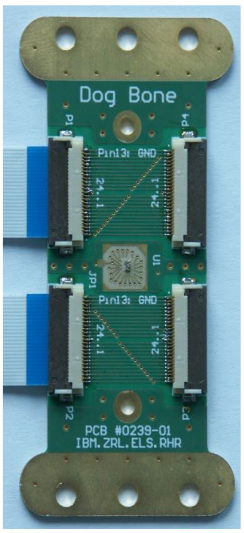


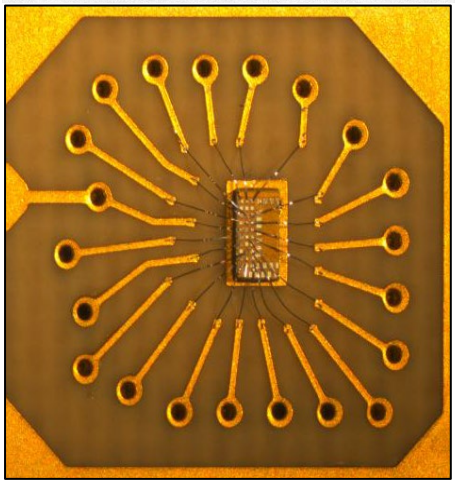
Fig. 2.19. I_{DS}-V_{GS} showing clear intersubband scattering effect (hump in I_{DS}) at the onset of the *front* channel for long NMOS GO1 LVT, when increasing FBB at 4.2K.

3 Extremely low temperature (20mK-4K) device characterization of III-V MOSFETS and 14nm FinFETs (contributor: IBM)

3.1 Measurement setup







3.1: (Left) Cross-section of a measured InGaAs-on-Si MOSHEMT. (Middle) Custom-made PCB holder for mK measurements. The test chip is mounted in the center area which is shown in the right-hand figure.

Two types of samples were prepared for the measurements: InGaAs-on-Si MOSHEMTs, as well as 14 nm FinFETs in commercial CMOS technology. The devices were on separate dedicated test chips with arrays of devices with various dimensions. Due to the low throughput of extremely low temperature measurements, and the need to wire-bond each measure device, a few representative devices were measured. The measurement cycle was about 3-4 days.

The measurements were done in a BlueFors bottom-loaded cryostat that reached 20-40 mK base temperature. The samples were mounted and wire bonded to a custom-made PCB holder. The PCB holder has enough outputs to measure about 3-4 devices in one measurement cycle.

The project has received funding from the European Union's Horizon 2020 research and innovation programme under Grant agreement number 871764 (SEQUENCE)

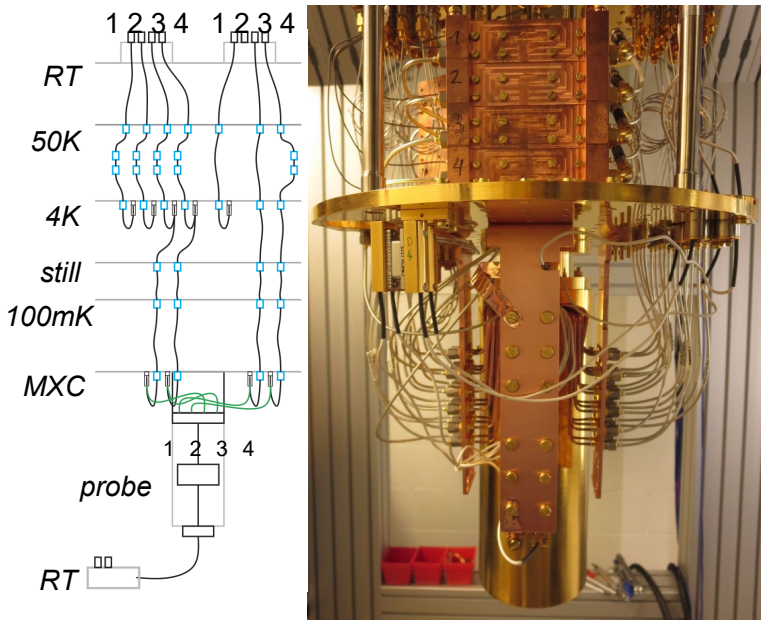


Figure 3.2: Schematic and photo of measurement setup.

Figure 3.2 shows a schematic of the measurement setup and wiring in the cryostat. Two types of cabling was available. High resistive cabling with RF and RC filters installed. The RF filter alone had approximately 2000 Ohm. Low-resistive/superconducting cabling was also available with 13 Ohms.

The cabling was tested with an on-chip resistor. Using the high-resistance cabling, a superconducting transition was measured at 2 K. With the superconducting cabling, we do not observe a superconducting transistor. An explanation for this behavior may be that the superconducting cables have infrared coupling that breaks superconductivity.

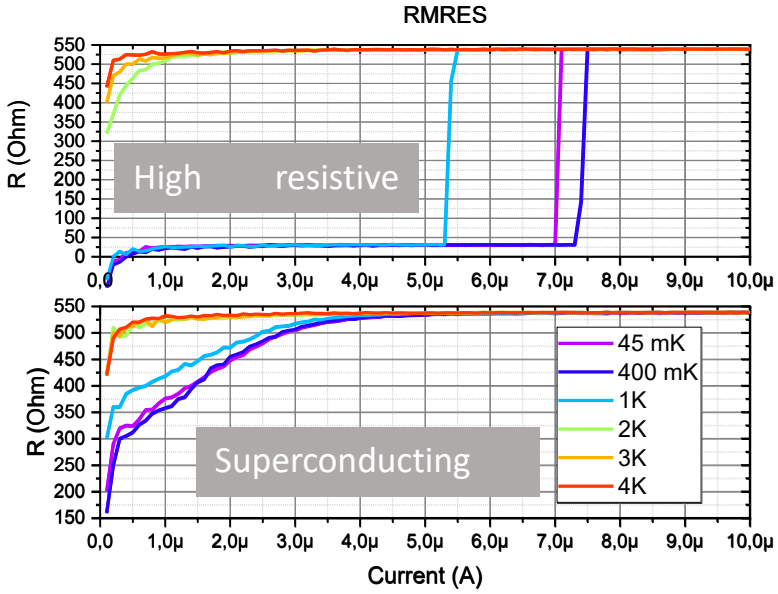


Figure 3.3 Measurements of a test resistor using high-resistance and superconducting cables.

3.2 Measurements of 14 nm FinFETs down to mK

NMOS and PMOS FinFETs with varying number of fins were measured down to about 40 mK. We note that measurements from room temperature to 4 K were done in a Janis cryogenic probe sta-

tion, while temperatures below that were measured in the BlueFors cryostat as described above. The threshold voltage of two 8 fin NMOS devices with different VT flavors is shown in Figure 3.4. As shown, the curve shows good continuity between the two measurement setups and a saturating behavior for temperatures below 10 K. This may be due to saturation of band gap widening at very low temperatures.

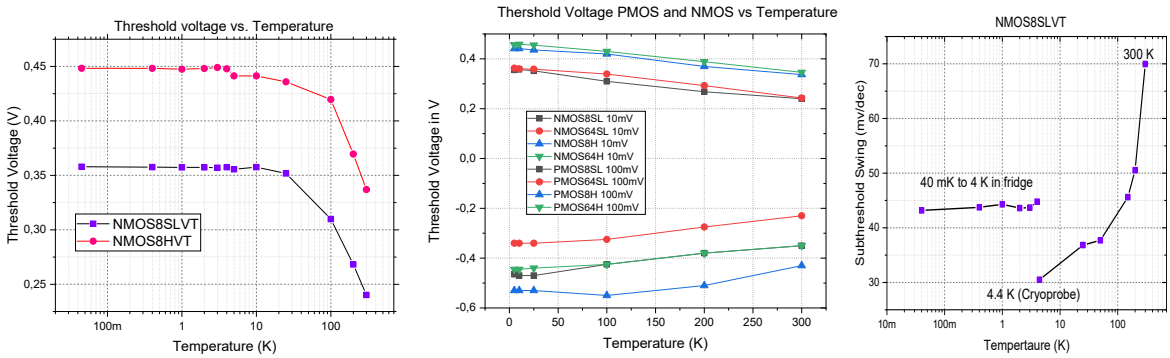


Figure 3.4 Measurements on 14 nm FinFET test chip down to 40 mK.

The subthreshold slope, however, shows a discontinuity between the measurement setups. One explanation could be the difference in cooling power available in these two setups. The cryo-prober is cooled with liquid He and has very large cooling power, while the mK fridge has a few 10 uW of cooling power. This could cause heating problems of the sample in the fridge, either due to self-heating or thermalization from wires.

We summarize the key findings from this study as follows:

- Below a certain temperature, doping impurities can freeze, but FinFETs are shown to work at 40 mK.
- Mobility increases, resulting in higher saturation drain current.
- Subthreshold slope increases, beneficial for low power circuit design.
- Ideal copper, wiring resistance decreases by 2 to 3 orders of magnitude. For on-chip wiring metal (Cu), resistance decrease is smaller but still of advantage (2-5x)
- Tungsten silicide resistors could become superconductive, somewhere below 4 K but we did not observe superconductivity in 14 nm.
- Temperature monitoring of the intrinsic device properties is challenging.
- ESD protection of the test devices is challenging.

3.3 Measurements of InGaAs MOSHEMTs down to mK

The InGaAs MOSHEMTs were measured using the same methodology. The measurement results are shown in Figure 3.5. Good continuity is found between the cryo-probe station and the dilution fridge.

As shown, transconductance increases at lower temperatures, from 0.35 mS/um at VDS = 100 mV, to 0.47 mS/um at the lowest temperature for the 20 nm gate length device. For the 50 nm gate length devices, instead transconductance goes from 0.35 to 0.58 mS/um. This significantly larger increase

for the longer gate length device may be due to quasi-ballistic transport. At lower temperatures the mobility increases due to reduced phonon scattering. This is equivalent to a longer mean free path between scattering events, λ. For drift-diffusion transport, i.e. when LG >> λ, the drain current is proportional to the mobility. When LG and λ of similar length, the device operates in the quasi-ballistic regime, in which case the drain current is no longer proportional to mobility of mean free path but rather to λ/(LG+λ). Effectively this means that a device in this regime with shorter gate length will exhibit less increase of the current and transconductance for higher values of mobility. This would be consistent with our observation.

For sub-Kelvin operation, all the shown device parameters saturate. We note that at these temperatures, even a slight increase of the channel temperature due to self-heating will dominate the ambient temperature. Therefore it may be that the measurements are probing a constant channel temperature due to self-heating.

The subthreshold slope values show some discontinuity between cryo-prober and dilution fridge. This may be the thermalization issue that was discussed before, and the fact that the subthreshold slope is likely the most sensitive parameter to the thermal exposure of the device. We show here also an InGaAs FinFET device with a single 20 nm wide fin in the same technology and on the same chip as the planar devices. This device shows signs of conductance quantization and exhibits extremely low subthreshold swing of 4 mV/decade.

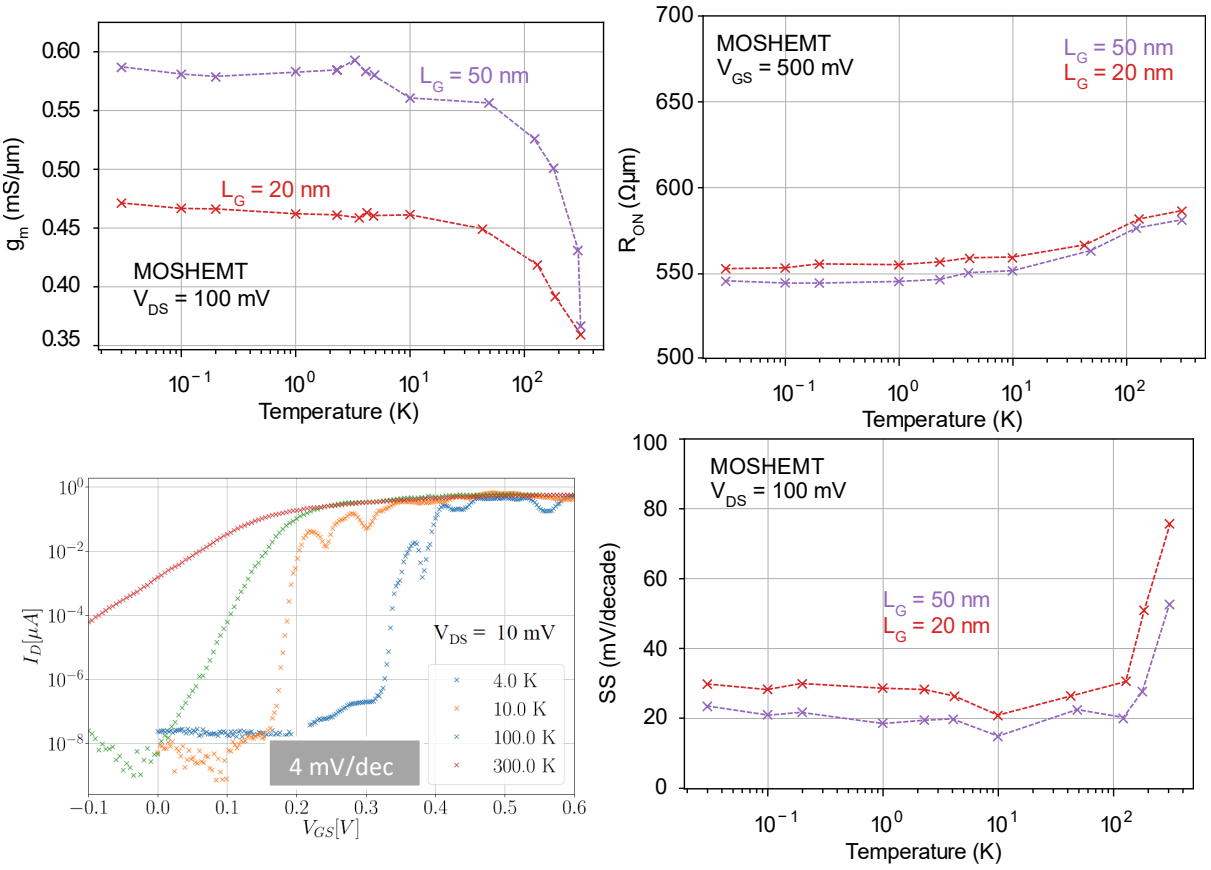


Figure 3.5 Measurements of InGaAs MOSHEMTs down to about 20 mK temperature.

4 Summary and conclusions

LETI has demonstrated for the first time that 28nm FD-SOI outperforms other CMOS technologies at low temperature. The use of addressable matrix for variability study was validated down 100mK, where such approach is likely the only reasonable solution for statistical investigation using dilution refrigerators. FBB promotes versatility over a wide T range of operation. Due to mobility and V_{TH} saturation below ≈20K, compact models comprising physical phenomena to describe FD-SOI operation at 4.2K should be valid down to 100mK. Relatively small degradation of V_{TH} and β variability are obtained at LT, which is encouraging for FD-SOI application in quantum computing. Finally, we presented first design guidelines and useful information for compact modelling and further design optimization for FD-SOI operating at deep cryogenic T.

IBM showed measurements at mK temperatures on InGaAs MOSHEMTs as well as commercial 14 nm FinFET devices. Extremely low temperature characterization is challenging for several reasons such as low throughput, increased effects of cabling and measurement setup, and increased sensitivity to self-heating. From the studies on the Si FinFETs, it was concluded that devices work all the way down to 40 mK without freezeout. This could in part be due to self-heating that thermalized dopants, in part due to all degenerately doped contact and spacer regions. The MOSHEMT devices showed significant increase of the transconductance, which was stronger in the longer channel devices. This could be a sign of quasi-ballistic transport. The results indicate that this transistor technology is well suited for sub-Kelvin operation.

5 References

section 2

[2.1] L. Hutin *et al.*, “All-Electrical Control of a Hybrid Electron Spin/Valley Quantum Bit in SOI CMOS Technology,” in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, pp. 125–126. doi: 10.1109/VLSIT.2018.8510665.

[2.2] E. Charbon *et al.*, “Cryo-CMOS for quantum computing,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 13.5.1-13.5.4. doi: 10.1109/IEDM.2016.7838410.

[2.3] H. Bohuslavskyi *et al.*, “28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing,” in *IEEE Silicon Nanoelectronics Workshop (SNW)*, 2017, pp. 143–144. doi: 10.23919/SNW.2017.8242338.

[2.4] S. Bonen *et al.*, “Cryogenic Characterization of 22-nm FDSOI CMOS Technology for Quantum Computing ICs,” *IEEE Electron Device Letters*, vol. 40, no. 1, pp. 127–130, 2019, doi: 10.1109/LED.2018.2880303.

[2.5] P. A. ’t Hart, J. P. G. van Dijk, M. Babaie, E. Charbon, A. Vladimircscu, and F. Sebastiano, “Characterization and Model Validation of Mismatch in Nanometer CMOS at Cryogenic Temperatures,” in *2018 48th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2018, pp. 246–249. doi: 10.1109/ESSDERC.2018.8486859.

[2.6] P. A. t Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, “Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures,” in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2019, pp. 98–101. doi: 10.1109/ESSDERC.2019.8901745.

[2.7] P. Galy, J. C. Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Pioro-Ladrière, "Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 594–600, 2018, doi: 10.1109/JEDS.2018.2828465.

[2.8] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electronics*, vol. 159, pp. 106–115, Sep. 2019, doi: 10.1016/j.sse.2019.03.033.

[2.9] H. Bohuslavskyi *et al.*, "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs described with Band Broadening," *IEEE Electron Device Letters*, pp. 1–1, 2019, doi: 10.1109/LED.2019.2903111.

[2.10] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 133–134. doi: 10.1109/VLSIT.2012.6242497.

[2.11] K. Triantopoulos *et al.*, "Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, doi: 10.1109/TED.2019.2919924.

[2.12] G. Ghibaudo *et al.*, "Electrical transport characterization of nano CMOS devices with ultra-thin silicon film," in *2009 International Workshop on Junction Technology*, Jun. 2009, pp. 58–63. doi: 10.1109/IWJT.2009.5166220.

[2.13] K. Triantopoulos, M. Cassé, L. Brunet, P. Batude, G. Reimbold, and G. Ghibaudo, "Self-heating assessment and cold current extraction in FDSOI MOSFETs," San Francisco, 2017. doi: 10.1109/S3S.2017.8309239.

[2.14] J. Mazurier, O. Weber, F. Andrieu, C. L. Royer, O. Faynot, and M. Vinet, "Variability of planar Ultra-Thin Body and Buried oxide (UTBB) FDSOI MOSFETs," in *2014 IEEE International Conference on IC Design Technology*, May 2014, pp. 1–4. doi: 10.1109/ICICDT.2014.6838617.

[2.15] E. G. Ioannidis, C. G. Theodorou, S. Haendler, E. Josse, C. A. Dimitriadis, and G. Ghibaudo, "Impact of Source–Drain Series Resistance on Drain Current Mismatch in Advanced Fully Depleted SOI n-MOSFETs," *IEEE Electron Device Letters*, vol. 36, no. 5, pp. 433–435, May 2015, doi: 10.1109/LED.2015.2411289.

[2.16] S. Mennillo, A. Spessot, L. Vendrame, and L. Bortesi, "An Analysis of Temperature Impact on MOSFET Mismatch," in *2009 IEEE International Conference on Microelectronic Test Structures*, Mar. 2009, pp. 56–61. doi: 10.1109/ICMTS.2009.4814610.

[2.17] M. Casse *et al.*, "Cryogenic Operation of Thin-Film FDSOI nMOS Transistors: The Effect of Back Bias on Drain Current and Transconductance," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4636–4640, 2020, doi: 10.1109/TED.2020.3022607.

[2.18] M. Cassé *et al.*, "Evidence of 2D intersubband scattering in thin film fully depleted silicon-on-insulator transistors operating at 4.2 K," *Applied Physics Letters*, vol. 116, p. 243502, 2020, doi: 10.1063/5.0007100.

section 4

[4.1] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 1: The Simplified EKV Model for the Design of Low-Power Analog Circuits," in *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26-35, 2017

[4.2] E. Memisevic, E. Lind, M. Hellenbrand, J. Svensson and, L.-E. Wernersson, "Impact of Band-Tails on the Subthreshold Swing of III-V Tunnel Field-Effect Transistor," in *IEEE Electron Device Letters*, vol. 38, no. 12, pp. 1661-1664, 2017

[4.3] E. Memisevic, M. Hellenbrand, E. Lind, A. R. Persson, S. Sant, A. Schenk, J. Svensson, R. Wallenberg, and L.-E. Wernersson, "Individual Defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect Transistors Operating below 60 mV/decade," Nano Letters 17 (7), 4373-4380, 2017

[4.4] S. Andrić, L. Ohlsson Fhager, O.-P. Kilpi, F. Lindelöw, and L.-E. Wernersson , “Low-temperature back-end-of-line technology compatible with III-V nanowire MOSFETs,” in Journal of Vacuum Science and Technology B (37), 061204 (2019), doi.org/10.1116/1.5121017

[4.5] *Processing Procedures for CYCLOTENE 3000 Series Dry Etch Resins*, DOW Chemicals, 2008, www.dow.com