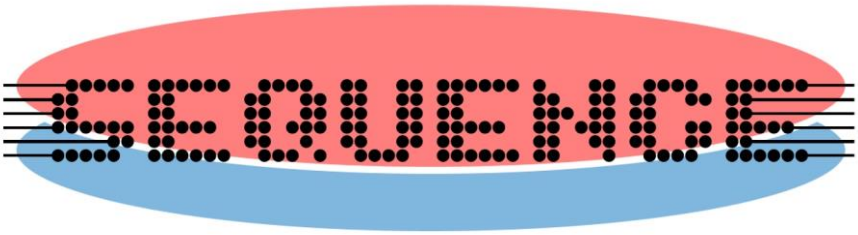
Deliverable – D2.3

First report on interface dielectric trap and RF (S parameter and NF) characterization of devices operated at cryogenic condition



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1 Introduction

The objectives of WP2 are i) to perform a detailed LF and RF electrical characterization and parameter extraction of the device operated under deep cryogenic conditions, and, ii) to develop associated LF and RF analytical compact device models valid at very low temperature and usable in circuit design simulation platforms. More specifically, Task 2 and Task 4 of WP2 aim at providing i) basic electrical characterization and improved parameter extraction, ii) insights into carrier transport properties (mobility, velocity) at very low temperature under degenerate statistics conditions for various devices (Si vs III-V) and iii) DC and RF electrical characterization of device operation at extremely low temperatures (20mK-4K) for physical understanding of device operation under deep cryogenic conditions for various Si and III-V devices.

The deliverable D2.3 due at M18 reports on first interface dielectric trap by C-V-f/G-V-f and LF noise characterization of III-V devices and FDSOI MOSFETs, as well as RF (S parameter and NF) characterization of III-V HEMT devices operated at deep cryogenic condition issued from industrial platform and from NW, TFET and III-V devices from WP1 consortium. More specifically, section 2 reports on cryogenic spectroscopy of border traps in III-V devices (Tyndall), section 3 deals with low frequency noise characterization of FDSOI MOSFET down to deep cryogenic temperatures (INPG/LETI), section 4 reports on RF characterization of III-V HEMTs operated at cryogenic conditions (IAF/FhG) and section 5 reports on pulsed IV characterization of nanowire MOSFETs at RT and 12 K (ULUND).

2 Cryogenic spectroscopy of border traps by C-G-V-f measurements and TCAD simulations in III-V devices (contributors: Tyndall)

2.1 Introduction

The thermal budget constraints associated with material systems such as III-V semiconductors or technology thermal limitations (e.g. monolithic 3-D integration) preclude the use of high-temperature thermal annealing to reduce oxide defect densities in the high-k oxides used in conjunction with alternative semiconducting channels. These constraints lead to defective oxides which cause device instabilities and introduce failure mechanisms driven by oxide defects. It is therefore imperative to introduce appropriate characterisation methodology for oxide defects (otherwise called border traps) and understand the physics behind their behaviour.

In this activity, a new methodology for border traps spectroscopy based on physics-based simulation of metal-oxide-semiconductor (MOS) systems will be presented and implemented on the high-k/InGaAs system at room temperature. The behaviour of border traps at cryogenic temperature is also investigated in this work.

2.2 Implementation of border traps spectroscopy at room temperature

For this study, 2 µm n-$In_{0.53}Ga_{0.47}As$ layer was grown lattice matched on an n+ InP (100) substrate by MOVPE using a nominal S doping concentration of $4x10^{17}$ cm^{-3} (confirmed by electrochemical C-V profiling). The test structures used in this section are MOS capacitors (MOScaps) where the Al_2O_3 dielectric was grown by atomic layer deposition (ALD). TEM measurements indicate an actual thickness of 6 ± 0.3 nm (Fig. 2.1). Ni(70 nm)/Au(90 nm) was used as the metal gate and was formed by electron beam evaporation and lift-off process. The MOScaps were thermally annealed post metal in forming gas ($0.05H_2/0.95N_2$) using the optimum temperature of 450 °C. It is important to note that MOScaps fabricated on p-$In_{0.53}Ga_{0.47}As$ as well as MOScaps using HfO_2 as a gate dielectric were fabricated in parallel and are also available for further investigations. These structures will be used in the second phase of SEQUENCE to bring more insight into the spectroscopy of border traps in the high-k/III-V system.

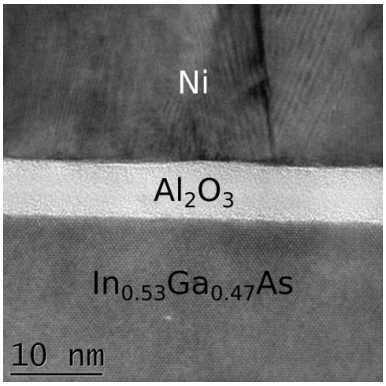


Fig. 2.1. Cross-sectional TEM image of a Au/Ni/Al_2O_3/InGaAs/InP MOScap. The gate oxide thickness is 6±0.3 nm.

The new defect spectroscopy method presented in this section is based on the accurate reproduction of experimental capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics using physics based simulations of the high-k/III-V MOScaps [2.1]. Commonly, the frequency dispersion from depletion to inversion (as observed in Fig. 2.3) is attributed to interface traps (ITs) response and the frequency dispersion in accumulation is attributed to oxide traps (OTs) aligned at, or above, the majority carrier band edge ('standard approach' of Fig.2.2 left) [2.2-2.7].

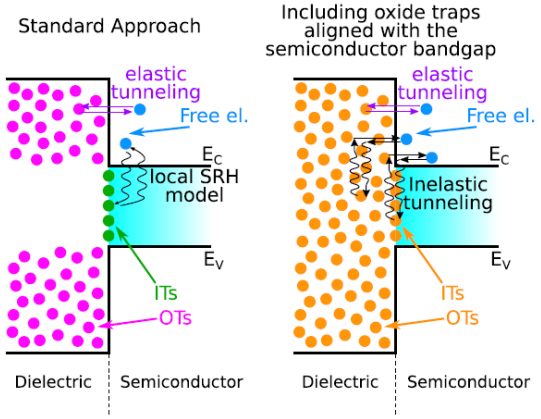


Fig. 2.2. MOS band diagram including defect and the possible trapping models. In the "standard" approach, the simulations rely on the inclusion of interface traps aligned with the semiconductor bandgap, that interact with the free carrier using the local SRH model, and oxide traps aligned with the conduction and valence band of the semiconductor, which communicate with the free carriers by elastic tunneling. In this work, OTs are included at any energy, including the semiconductor bandgap. Carriers communicate with defect through a nonlocal NMP model both elastic and inelastic tunneling.

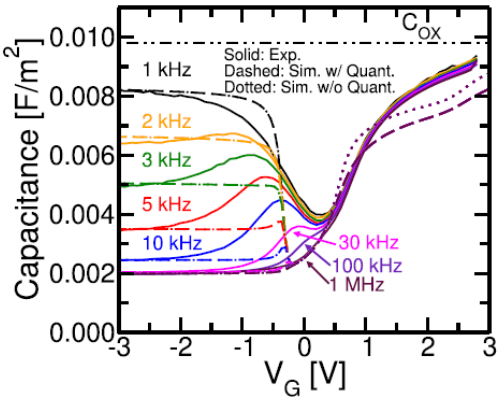


Fig. 2.3. Experimental multifrequency C-V (solid lines) at 300K compared with ideal simulations (without traps). Simulations obtained with/without quantization for electrons are reported with dashed and dotted lines, respectively.

However, using this approach it is difficult to accurately reproduce the full C-V /G-V responses through simulations [2.3]. In particular, the frequency-dependent "humps" in the region of weak inversion cannot be fitted without a large electron capture time response of interface traps with energy close to the InGaAs valence band edge [2.4], [2.6]. The main limitation of this method is the attempt to explain the capacitance and conductance frequency dispersion in depletion using only interfacial states [2.2], without providing a full-physical description of the carrier capture/emission

process, which has to include both the tunneling through the dielectric barrier and the lattice relaxation at the interface/border trap sites. The new approach (Fig 2.2 right) presented here includes oxide traps energetically aligned with the semiconductor bandgap and a nonlocal model to describe capture and emission from interface defects when inversion layer quantization effects are considered in the physical simulation.

The simulations are done in a commercial TCAD environment [2.8] and include Fermi-Dirac statistics and multivalley/nonparabolic band structure. Generation-recombination processes governing carriers' transitions between conduction and valence bands are modelled using the Shockley-Read-Hall (SRH) theory. Quantum corrections of the carrier density are considered using the modified local density approximation (MLDA) [2.9]. The interface traps distribution ($D_{IT}(E)$ in [$cm^{-2}eV^{-1}$]) is considered in simulations using the SRH extended formalism for phonon-assisted recombination at defects in semiconductor devices. For the case of oxide traps, the models for the interaction of the defects with free carriers in the semiconductor conduction and valance bands require sophisticated models accounting for the tunneling process [2.10], where the charge exchange between oxide states and the channel occurs via a multiphonon rather than an elastic tunneling process [2.10], [2.11]. The simulations presented here employ the inelastic nonlocal band-to-trap tunneling model used in [2.13], which relies on the nonradiative multiphonon (NMP) theory [2.10], [2.12]. In the NMP model, the electrically active defect is described by a trap volume V_T, the Huang-Rhys factor S, the phonon energy $\hbar\omega$, the tunneling mass m_t, and either a trap level localized in energy and space $E_{T,z}$ or a distribution of levels D_{OX}. The Huang-Rhys factor S is linked to the relaxation energy (E_{REL}) of the defect through the relation $E_{REL} = S\,\hbar\omega$. It represents the energy that is required for the lattice relaxation process to occur [2.13], [2.14], and determines the capture and emission time constants and their temperature dependence. Moreover, it can be useful to identify the physical nature of the defects. The expected value for the Al_2O_3 phonon energy is ~50 meV [2.15], [2.16] and the Huang-Rhys factor reported in the literature is around 12 [2.17], [2.18]. V_T is chosen to be 10^{-23} cm^3, whose edge corresponds to the radius on an IT with a circular capture cross section σ of 1.46×10^{-15} cm^2, a typical value used for interface and oxide defects.

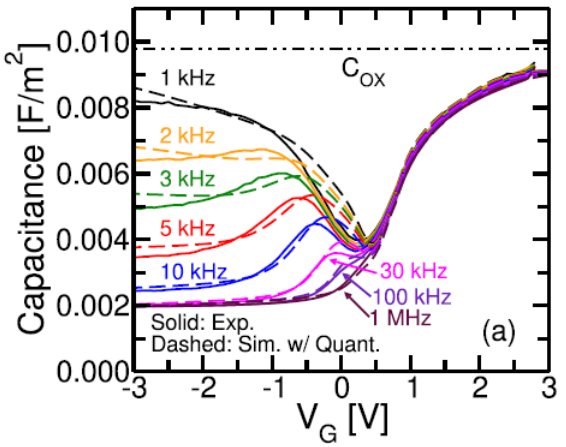


Fig. 2.4. Experimental (solid lines) multi-frequency C-V and (b) G-V compared with simulated data (dashed lines), including quantization correction and nonlocal model for traps. Simulations use the $D_{OX}(E,z)$ shown in Fig. 2.5.

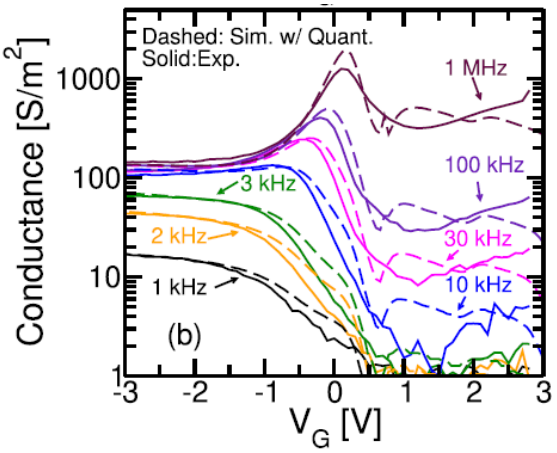


Fig. 2.5. Experimental (solid lines) multi-frequency G-V compared with simulated data (dashed lines). The G-V simulations include the $D_{OX}(E,z)$ extracted to reproduce the experimental C-V of Fig.2.4. No parameter adjustment was required to accurately predict the experimental G-V.

Fig 2.3 shows that the experimental C-V response deviate from the ideal simulation. It is instructive to first consider the multifrequency C-V characteristics of the ideal InGaAs MOS structure and the effect of the quantization model for electrons (dashed and dotted lines in Fig. 2.3). As expected, quantization reduces the accumulation capacitance in devices with thin oxides due to the shift of the charge centroid from the interface. The deviation between the experiments and the ideal (no traps) case is significant and is due to the ac and dc response of electrically active defects in the measured structures.

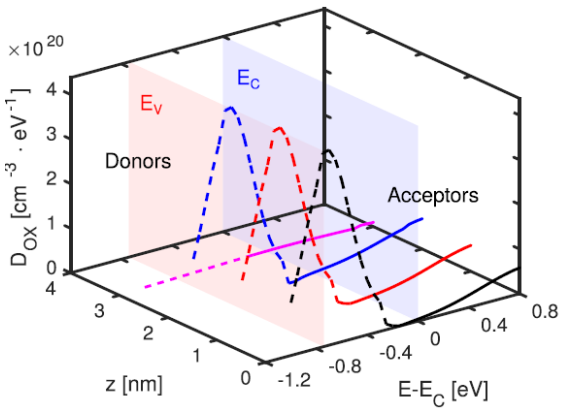


Fig. 2.6. $D_{OX}(E,z)$ inside the Al_2O_3 of donor and acceptor traps used in simulations of Fig. 2.4 and 2.5. The energy distributions are referred to the InGaAs conduction band edge (E_C). It is noted that the density of donor states aligned with the InGaAs bandgap, and the acceptor states at energies above E_C, both exhibit a gradual increase with depth into the oxide (z).

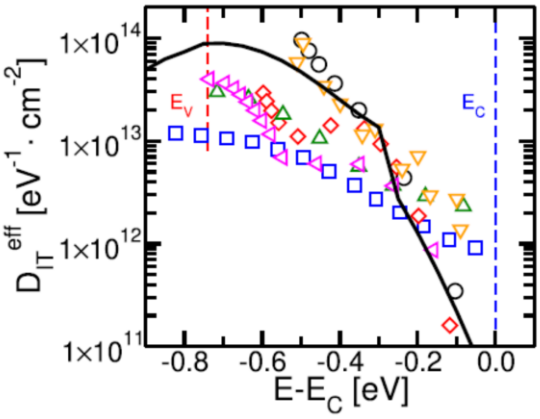


Fig. 2.7. Comparison between the effective $D_{IT}^{eff}(E)$ obtained from Fig. 2.6. by the projection of all the electrically active traps at the semiconductor/oxide interface (black solid line) and the $D_{IT}^{eff}(E)$ reported in the literature extracted from different devices and using standard extraction method based on C-V and G-V response. The energy distributions are referred to the InGaAs conduction band edge (E_C). ○ [2.3] □ [2.6] ◇ [2.19] △ [2.20] ◁ [2.21] ▽ [2.22]

The simulated C-V response is shown together with the experimental response in Fig. 2.4, where the results have been obtained by considering the $D_{OX}(E,z)$ distribution shown in Fig. 2.6 and a nonlocal model for electron and hole interaction with oxide defects. It is important to note that this fit to the experimental data is achieved using only oxide traps which extend to the oxide/InGaAs interface. No specific distribution to represent $D_{IT}(E)$ is included at the interface (z = 0). By assuming the same oxide trap distribution used in Fig. 2.4 the corresponding G-V response (Fig. 2.5) is predicted with remarkable accuracy and without any adjustment of the simulated parameters, suggesting again the congruity of the approach and the physics. The agreement between simulations and experiments is good, although second-order adjustments on D_{OX} may allow us to further improve the agreement. The inclusion of the OTs aligned to the InGaAs bandgap and extended up to the surface (z = 0) and without any need of an additional $D_{IT}(E)$ has improved the agreement in the transition between depletion to weak inversion capacitance and conductance, which has not previously been achieved to this extent [2.3].

It must be stressed that in the standard extraction method based on C-V and G-V response [2.7], i.e., Terman, high-low frequency, and conductance methods, all deviations from the ideal C-V/G-V response are interpreted as ITs. As a result, these techniques yield an effective $D_{IT}^{eff}(E)$ which consists of conventional ITs, in addition to a projection to the semiconductor/oxide interface of all oxide traps in the oxide which can respond to the dc sweep and the ac signal at a given frequency. To illustrate this point, Fig. 2.7 shows the effective IT distribution $D_{IT}^{eff}(E)$ obtained by spatial integration of

D_{OX} at flat-band condition (no band bending), weighing the contribution of each trap in the oxide in such a way it has the same electrostatic effect of a trap placed at the interface (z = 0), that is,

$$D_{IT}^{eff}(E) = \int_0^{tox} [D_{OX}(E,z)(t_{ox} - z)/t_{ox}]dz$$

These results are fairly consistent with our present work, but they do not provide the spatial distribution of defects into the oxide.

2.3 Characterisation of border traps at cryogenic temperature

In this activity, high-k/III-V MOScaps impedance is measured from room temperature down to cryogenic temperature. Impedance spectroscopy as a function of temperature will provide further insight into the physical mechanisms governing the behaviour of defects in the gate oxide and ultimately inform how oxide traps affect device operation at cryogenic temperature.

Previously published cryogenic studies of III-V MOScap impedance focused mainly on the evolution of capacitance frequency dispersion in strong accumulation as a function of temperature [2.23], [2.24]. In contrast, the approach adopted in this work will exploit the C-V and G-V characteristic across the full voltage range.

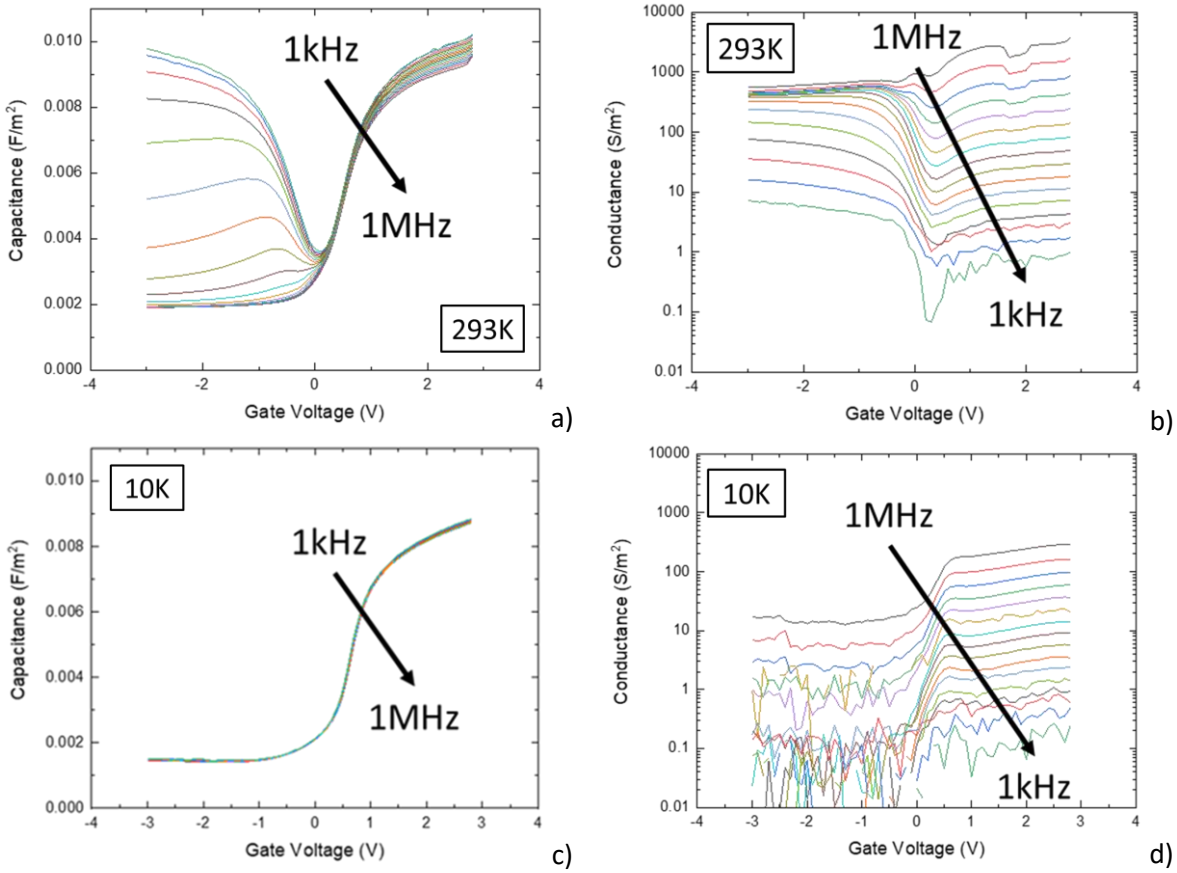


Fig. 2.8. Multi-frequency C-V and G-V characteristics measured at room temperature a) and b) and at 10K c) and d) on an Au/Ni/Al_2O_3/InGaAs/InP MOScap.

The cryogenic data presented in this section were obtained on a sample identical to the Au/Ni/Al_2O_3/InGaAs/InP structures used in section 2.2 except for the FGA thermal treatment, which was performed at 300°C instead of 450°C. The room temperature and the 10K C-V and G-V measurements are compared in Fig. 2.8. The frequency dispersion dramatically reduces in all the C-V re-

gions from depletion to accumulation. The minority carrier response in inversion is controlled by either generation through mid-gap states in the space charge region or carrier diffusion from the neutral region, which are both thermally activated processes and are expected be suppressed at 10K. In accumulation, the frequency dispersion, as discussed in section 2.2, is caused by free majority carriers communicating with traps in the oxide. We have seen that the inelastic band-to-trap tunneling model involving a non-radiative multi-phonon process describes accurately the measured characteristics at room temperature. The frequency dispersion reduces from ~2% (per decade frequency) at 293K to 0.4% at 10K. This significant reduction confirms the thermally activated component of capture and emission by oxide traps.

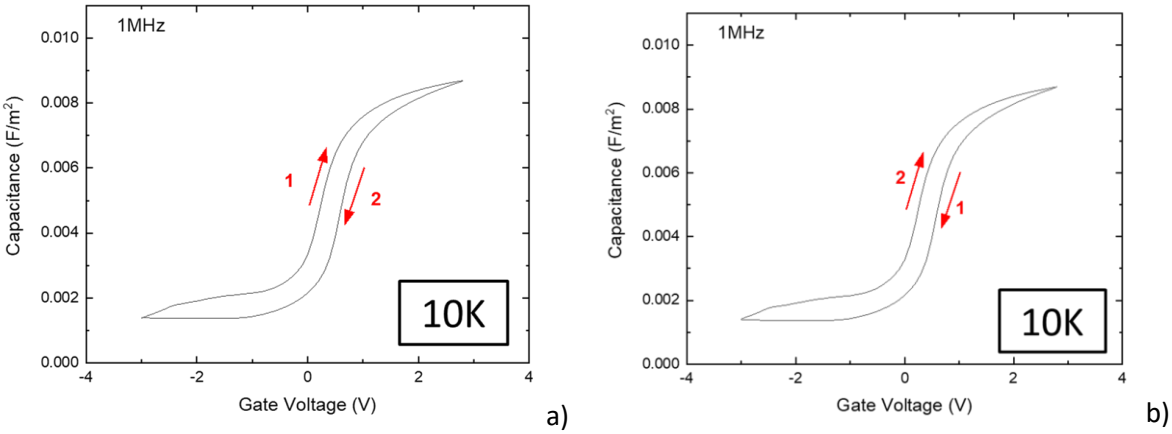


Fig. 2.9. 10K C-V hysteresis characteristics measured from depletion to accumulation and back a) and from accumulation to depletion and back. The time between the two measurements a) and b) was kept at minimum. The successive characteristics are identical showing that (assuming it is charge trapping) injected charges in the first sweep can be recovered after the one.

C-V hysteresis measurements can also be used to investigate oxide defects in MOScaps. It was shown that C-V hysteresis and the frequency dispersion of capacitance in accumulation at room temperature are correlated [2.25]. The C-V characteristics measured at 10K (Fig. 2.9), however, present an unexpected result with a significant hysteresis window equivalent to a $2x10^{12}$ cm^{-2} sheet charge at the interface, which is higher than the measured value at room temperature. The hysteresis window is expected to reduce at 10K or at least reduce upon successive sweeps as there isn't enough thermal energy at 10K for the injected charge be recovered.

Further analysis is required to elucidate if the observed hysteresis at 10K could be caused by effects other than charge trapping in border traps.

The methodology presented in section 2.2 provides a very detailed oxide defect distribution extracted at room temperature using fully-physics based model as opposed to distributed RC circuit models [2.24], which do not include important physical parameters. Future effort in the second phase of Sequence will be to test the developed defect model at different temperatures and attempt to predict the measured C-V and G-V data down to cryogenic temperature. It is also planned to investigate the properties of available twin p-type InGaAs structures at cryogenic temperature to help understand the different trends in capacitance hysteresis and frequency dispersion with temperature. The proposed approach of section 2.2 will also be implemented to extract the energy and depth distribution of OTs in the HfO_2/InGaAs system.

3 Low frequency noise characterization of FDSOI MOSFETs down to deep cryogeic temperature (contributor: LETI/INPG)

3.1 Introduction

The interest in cryogenic electronics relies on several applications, such as space and cooling systems [3.1], [3.2], and has been recently boosted by the quantum computing field [3.3], [3.4]. Recently, monolithic integration between qubits and readout circuitry has been demonstrated at 2 K in 22-nm fully-depleted silicon-on-insulator (FDSOI) technology [3.5] and the electrical performance of several CMOS technologies has shown to be significantly improved with temperature T decrease [3.6]–[3.8]. On the other hand, in [3.9], it is indicated that the low-frequency noise (LFN) to signal power increases at cryogenic T, especially in the presence of subband scattering mechanisms [3.10]. Moreover, in [3.11], the authors claim that low-frequency charge noise is one of the key parameters to improve qubit fidelity in Si spin qubits.

To our knowledge, the performance of 22/28-nm FDSOI MOSFETs at deep cryogenic temperatures has not been explored yet, especially regarding the device optimization by means of forward back biasing (FBB). Furthermore, there is a lack of information on LFN behaviour at cryogenic temperatures available in literature for commercial technologies. In this work, our goal is to cover the abovementioned topics, concerning advanced FDSOI MOSFET characterization at 4.2 K, with special focus on the origin of LFN down to 4.2 K and the underlying physics.

3.2 Experimental details

Si nMOSFETs and SiGe (with Ge content around 25%) pMOSFETs fabricated with gate-first high-k metal gate integration in commercial 22-nm FDSOI CMOS technology [3.12] were evaluated in this work. The undoped semiconductor channel is about 6-nm thin, whereas the buried oxide thickness is 20 nm, and the equivalent oxide thickness (EOT) is around 1.3 nm. Experimental measurements were performed down to 4.2 K using a manual cryogenic probe station. Fast IV module B1530A from Agilent was used for LFN characterization through time-domain current sampling measurements [3.13]. For spectral analysis, Welch function was used to apply the Fourier transform and obtain the power spectral density.

3.3 Static performance versus Temperature

Fig. 3.1 presents the drain current I_{DS} as a function of the gate voltage V_{GS} at high and low drain bias V_{ds}, for nMOS and pMOS, down to 4.2 K. Temperature lowering leads to expected threshold voltage V_{TH} and I_{DS} increase, in absolute values, for both nMOS and pMOS. As T decreases, the balance between mobility increase and V_{TH} shift toward higher absolute value originates the zero-temperature coefficient (ZTC). Since the T -dependence of V_{TH}, $|\Delta V_{TH}/\Delta T|$ is higher for pMOS (≈0.71 mV/K, in comparison with ≈0.57 mV/K for nMOS), larger V_{DS} dependence is found for V_{ZTC} [3.14].

Fig. 3.2(a) shows V_{TH} as a function of T for nMOS at V_{DS} = 50 mV and 0.9 V, and at back gate bias V_B of 0 and 1.4 V. The applied 1.4 V at the back bias gives the same V_{TH} value as for the device operating at room temperature. Fig. 3.2(b) indicates the V_B required to shift V_{TH} back to its value at 300 K for each temperature operation. FBB is an efficient way to correct the significant V_{TH} increase with T

lowering and, therefore, enhance power efficiency. The measured drain-induced barrier lowering (DIBL) is ≈74 mV/V at both conditions, at 300 K with V_B=0 V and at 4.2 K with V_B=1. 4 V.

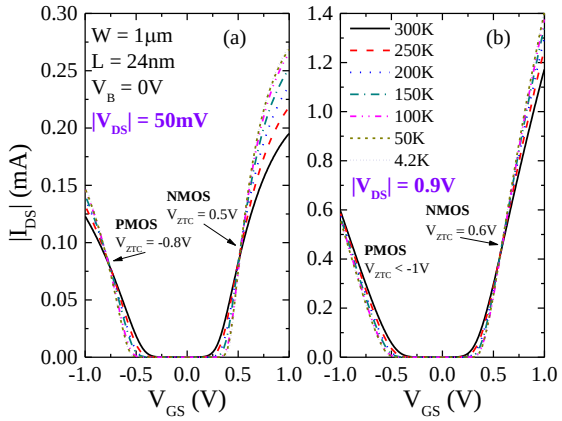


Fig. 3.1. $|I_{DS}|$ *versus* V_{GS} at $|V_{DS}|$ = 50mV (a) and 0.9V (b), for N- and PMOS, varying T from 300K to 4.2K.

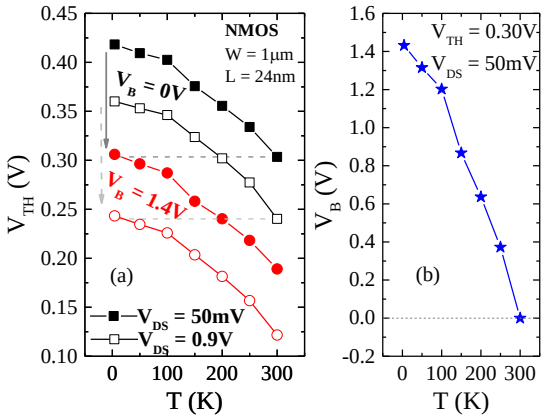


Fig. 3.2. V_{TH} *versus* T at V_{DS} = 50mV and 0.9V, and at V_B = 0V and 1.4V (a). V_B needed to shift V_{TH} back to its value at 300K for each temperature operation, at V_{DS} = 50mV (b).

Fig. 3.3(a) presents V_{TH} as a function of V_B for short-channel nMOS and pMOS at 300 and 4.2 K. The back bias efficiency, evaluated through the body factor ($\gamma = \Delta V_{TH}/\Delta V_B$), does not change with T. This is because the doping concentration of the back planes in ultrathin body and buried oxide MOSFETs is high enough to be always activated, so devices do not suffer from any freeze-out effect [3.15], which could reduce $|\gamma|$ at low T. Fig. 3.3(b) shows γ as a function of T for nMOSFETs and pMOSFETs with three different channel lengths, L = 24 nm, 70 nm, and 1 μm. Fig. 3.3(b) confirms that γ is T-independent, since $\Delta\gamma/\Delta T$ < 5% for all studied devices. Therefore, the back bias remains a powerful tool down to cryogenic T and can still be used to facilitate circuit design [3.16]. We can observe slightly lower $|\gamma|$ as the channel length becomes shorter, likely due to stronger influence of source and drain potentials inside the channel in shorter transistors. The difference between γ in nMOS and pMOS is expected since the position of the inversion layer in the channel (centroid of charges) differs according to the type of carriers (hole versus electron) and channel material (SiGe versus Si) [3.17].

Fig. 3.4(a) shows the ON-state current (I_{ON}) as a function of T for nMOS at V_{GS} = V_{DS} = 0. 9 V and varying V_B. The I_{on} gain observed with T decrease is attributed to the effective mobility increase due to suppression of phonon scattering contribution [3.18], whereas the I_{on} gain with FBB is the consequence of the V_{TH} shift, and thus gate which increases the gate voltage overdrive (V_{GT}=V_{GS}–V_{TH}). Fig. 3.4(b) shows I_{on} normalized by I_{on} extracted at 300 K and no back bias, $I_{on}/I_{on,\,ref}$, as a function of T for short and long nMOSFETs. The I_{on} gain with T reduction and FBB is higher for the long channel MOSFET in comparison with short channel one. This could be explained by the fact that shorter MOSFETs suffer from stronger self-heating effect [3.19], due to higher normalized input power, and also from larger access resistance impact and stronger contribution of T-independent transport mechanisms, related to neutral defect scattering and/or ballistic effect [3.20].

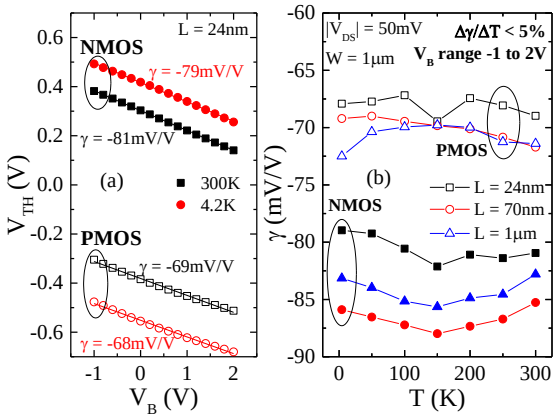


Fig. 3.3. V_{TH} *versus* V_B (a) and γ *versus* T (b) for N- and PMOS, at $|V_{DS}|$ = 50mV.

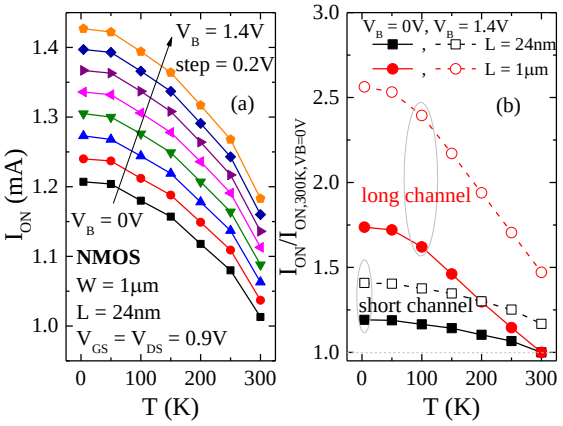


Fig. 3.4. I_{ON} *versus* T for NMOS, at V_{GS} = V_{DS} = 0.9V, and varying V_B (a). $I_{ON}/I_{ON,ref}$ *versus* T for long and short channels NMOS, at V_{GS} = V_{DS} = 0.9V, and at V_B = 0V and 1.4V (b).

Fig. 3.5(a) and (b) shows the maximum transconductance ($g_{m,peak}$) and the respective cutoff frequency ($f_{T,peak}$) as a function of T. The $f_{T,peak}$ values in this work were calculated from $g_{m,peak}/(2\pi . C_{ox} W.L)$ where C_{ox} = 0.028 F/m² is the oxide capacitance per unit area. Results are very similar to those obtained using RF characterization in [3.12], at 300 K. Curves are presented for two bias configurations, at fixed V_B = 0 V and at V_B required to keep V_{TH} constant at its value obtained at 300 K ($V_{TH,300K}$). A very small V_B impact on $g_{m,peak}$ (around ≈3%) is observed for the short channel transistors in Fig. 3.5, while for long channel MOSFETs, FBB is found to improve $g_{m,peak}$ results in a more significant way (up to +11%, not shown). This indicates that power consumption optimization can be achieved by means of back biasing, while >450 GHz cutoff frequency is kept. Moreover, we clearly observe the $g_{m,peak}$ (and therefore $f_{T,peak}$) improvement with T lowering for both nMOS (up to 38%) and pMOS (up to 16%). The results obtained in this work for 22-nm FDSOI are benchmarked against 28-nm bulk CMOS technology [3.6]. Regular-V_{TH} nMOS (RVTn) and high-V_{TH} pMOS (HVTp) flavors from [3.6] were chosen for comparison to match similar V_{TH} to our devices, as indicated in Table 3.1. From the $f_{T,peak}$ values in Fig. 3.5(b), it is observed that FDSOI outperforms bulk technology, especially for the nMOSFET, where a large $g_{m,peak}$ gain is obtained at cryogenic temperatures.

Table 3.1. Extracted Threshold voltage.

	22nm FDSOI – this work		28nm Bulk – [3.6]	
	NMOS	PMOS	NMOS	PMOS
300K	0.24V	-0.33V	0.26V	-0.37V
7K	0.36V	-0.50V	0.35V	-0.45V

Fig. 3.6(a) and (b) presents $I_{DS}(V_{GS})$ for a short device measured in four different dies at 4.2 K and the subthreshold swing $SS=\Delta V_{GS}/\Delta(\log I_{DS})$ as a function of the normalized current at 300 and 4.2 K. At room temperature operation, the subthreshold swing can be easily extracted. At cryogenic temperatures, the appearance of oscillatory regime likely due to quantum interference in the subthreshold region complicates the SS extraction at 4.2 K, given the strong dependence of this parameter on the current level used for the extraction. As shown in Fig. 3.6(a), this phenomenon presents

high variability. The extracted ideality factor (η) is ≈1.22 at 300 K, and more than 10 at 4.2 K, which cannot be explained by an increase of the interface trap density, but the appearance of an exponential tail of states in the subband, as discussed in [3.21] and [3.22], which leads to the SS saturation versus T below ≈50 K. From a performance point of view, even though the experimental SS is much higher than the theoretical limit at 4.2 K (SS≈0.8 mV/dec), it induces an OFF-state current (I_{OFF}) reduction of several orders of magnitude in comparison with the room temperature operation, lying below the equipment accuracy (1 fA).

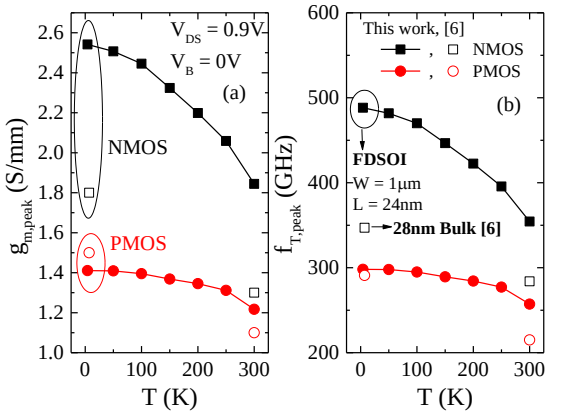


Fig. 3.5. $g_{m,peak}$ *versus* T (a) and $f_{T,peak}$ *versus* T (b) for N- and PMOS, at V_{DS} = 0.9V, and at V_B = 0V.

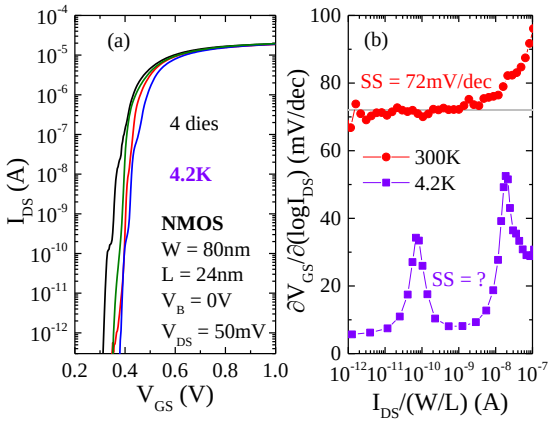


Fig. 3.6. I_{DS} *versus* V_{GS} (a) and $\partial V_{GS}/\partial(\log I_{DS})$ *versus* $I_{DS}/(W/L)$ (b) for short channel NMOS, at V_{DS} = 50mV.

3.4 LF Noise in 22nm FDSOI devices

Fig. 3.7(a) and (b) presents the normalized drain current power spectral density (S_{ID}) as a function of frequency (f), varying T, in linear and saturation regimes. From 300 down to 4.2 K, both nMOSFET and pMOSFET (not shown) exhibit 1/f noise behaviour. Moreover, S_{ID}/I_{DS}^2 increases with temperature reduction. In order to identify the sources of noise and explain its behaviour with T, S_{ID}/I_{DS}^2 values at 10 Hz are presented as a function of I_{DS}, from moderate to strong inversion in Fig. 3.8. The lines indicate the carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) analytical model given by,

$$\frac{S_{Id}}{Id^2} = S_{Vfb}\left(\frac{gm}{Id}\right)^2\left(1+\Omega\frac{Id}{gm}\right)^2 \qquad (3.1)$$

where $\Omega=\alpha_c.\mu_{eff}.C_{ox}$ is a noise parameter related to the Coulomb scattering coefficient (α_c) and $S_{Vfb}=q^2.\lambda.kT.Nt/(W.L.C_{ox}^2.f)$ is the flat band voltage power spectral density related to the slow oxide states (border trap) volume density N_t, with λ being the tunneling constant in the dielectric (≈0.1nm) [3.23]. Since good agreement between the data and the model is obtained from 300 down to 4.2 K, we can conclude that CNF and CMF are the sources of noise, and the 1/f noise-to-signal power increases with T lowering because of the g_m/I_{DS} improvement, on the same way as previously found for bulk CMOS [3.24]. Moreover, as the 1/f noise decays with exponent equal to 1, it means that the oxide traps are mostly uniformly distributed in depth, inside the gate oxide.

Results of S_{Vfb} were extracted using Eq. (1) in Fig. 3.8, for nMOS and pMOS. For all T conditions, Ω is found to be constant and equal to $4V^{-1}$. We can observe, in Fig. 3.9(a), that S_{Vfb} values are roughly constant with T. The same behavior is verified for the calculated oxide trap density, N_t, normalized by $1/kT$ in Fig. 3.9(b). Fig. 3.9(c) shows a large increase of the active trap density at cryogenic tem-

peratures. This could be because the accessed energy distribution gets closer to the conduction (for nMOS) and valence (for pMOS) bands as T reduces. Therefore, the high N_t values obtained at 50 and 4.2 K could be explained by the existence of the disorder-induced exponential tail at the subband edges, where the Fermi level lies at very low temperatures [3.25]. However, this explanation could be questionable when going to extreme low temperatures, while T tending to zero would lead to infinitely large N_t values. This could reveal the limit of validity of the fluctuation-dissipation theorem at zero temperature, where pure elastic tunnelling would dominate.

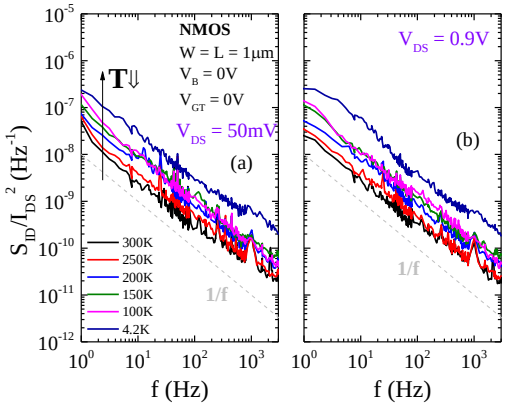


Fig. 3.7. S_{ID}/I_{DS}^2 *versus* f for NMOS, varying T, at V_{GT} = 0V and at V_{DS} = 50mV (a) and 0.9V (b).

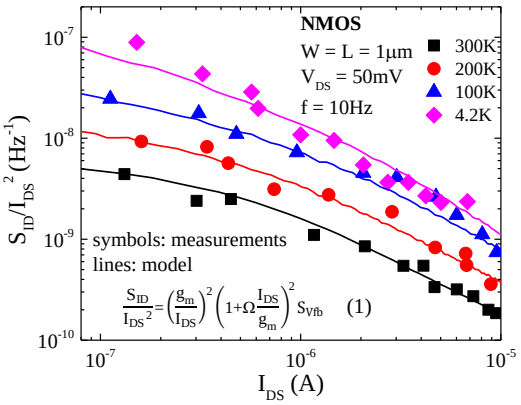


Fig. 3.8. S_{ID}/I_{DS}^2 *versus* I_{DS} for NMOS at different T conditions, $|V_{DS}|$ = 50mV, and at f = 10Hz. Lines indicate the CNF/CMF model [3.18]. Ω = $4V^{-1}$.

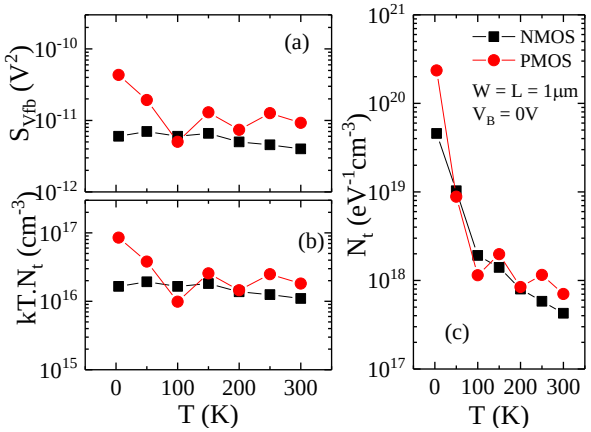


Fig. 3.9. S_{Vfb} (a), $kT.N_t$ (b) and N_t (c) *versus* T for N- and PMOS. $N_t = S_{Vfb}.W.L.f.C_{ox}^2/q^2.\lambda.kT$.

3.5 LF noise in 28nm FDSOI devices

Additional LF noise measurements were performed on 28nm FDSOI nMOS devices in order to analyse the influence of the back bias on the noise level. The measurements were performed on 28nm FDSOI nMOSFETs with silicon film thickness t_{si}=7nm and buried oxide (BOX) thickness t_{box}=25nm from STMicroelectronics. NMOS transistors were processed from (100) handle substrate, with <100>-oriented channel, and a high-k/metal gate Gate-First architecture [3.26]. Low-V_{th} transistors were available with un-doped channel through a doped back plane (NWELL doping $N_A=10^{18}cm^{-3}$) below the BOX. Thin gate oxide (with equivalent oxide thickness EOT=1.1nm) devices with gate length L=300nm and with gate width W=1µm were tested using a cryogenic probe station down to 77K. Fast IV module B1530A from Agilent was used for LFN characterization through time-domain

current sampling measurements. For spectral analysis, Welch function was used to apply the Fourier transform and obtain the power spectral density.

Typical spectral densities of drain current are illustrated in Fig. 3.10 for various gate voltages and indicating a 1/f noise behaviour for such geometry at 77K. The variations of the normalized power spectral density of drain current, Sid/Id^2 versus drain current from weak to strong inversion are shown in Fig. 3.11 for a given frequency (f=10Hz) and various back biases measured at 150K. As in section 3.5, the LF noise data are also well fitted with the CNF/CMF LF noise model of Eq. (3.1). The variations of the extracted flat band voltage spectral density S_{Vfb} and associated border trap volume density N_t are shown in Figs 3.12 and 3.13. As can be seen from the figures, S_{Vfb} and N_t are not significantly depending on the back bias, even though the back channel is strongly inverted at V_b=4V. This feature indicates that the LF fluctuations are still dominated by trapping-detrapping of carriers at the front interface, though the BOX bottom interface plays a role in the back channel operation.

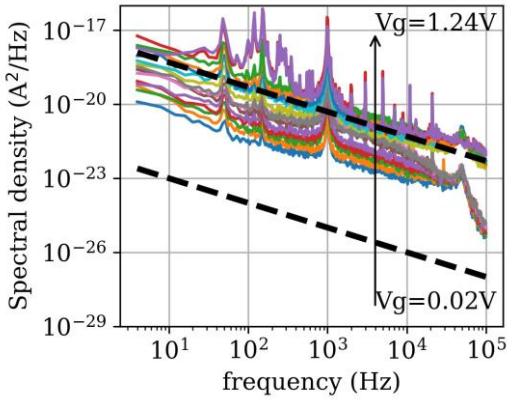


Fig. 3.10. Drain current spectral density for various front gate voltage measured at 77K (Vd=0.05V, Vb=0V).

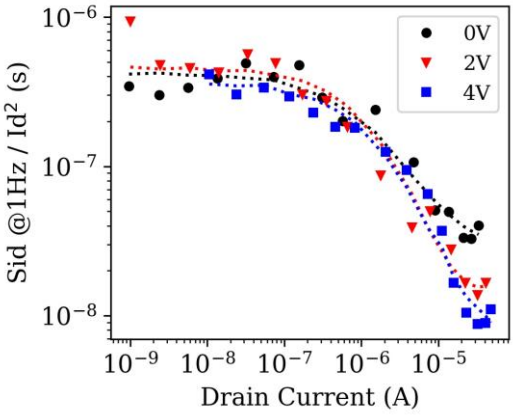


Fig. 3.11. Sid/Id^2 vs drain current Id for various back biases Vb measured at 150K (Vd=0.05V, f=10Hz).

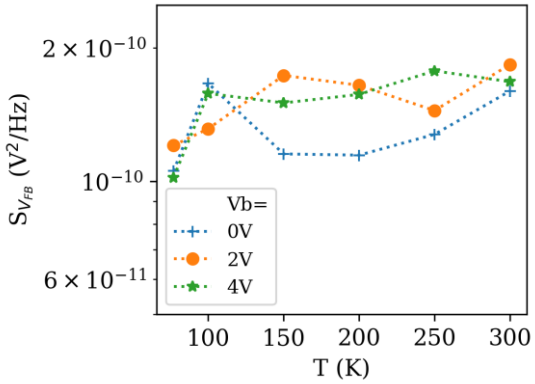


Fig. 3.12. Variations of SVfb with temperature as extracted with CNF/CMF model.

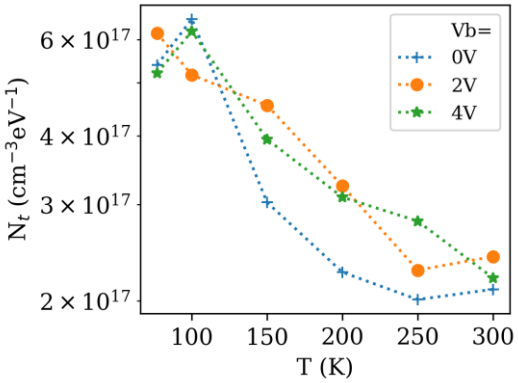


Fig. 3.13. Variations of volume border trap densty Nt with temperature. $N_t = S_{Vfb}.W.L.f.C_{ox}^2/q^2.\lambda.kT$, where λ is the tunneling constant in the dielectric (≈0.1nm).

4 RF (S-parameter and NF) Characterization of III-V HEMTs Operated at Cryogenic Conditions (contributor: Fraunhofer IAF)

4.1 Introduction

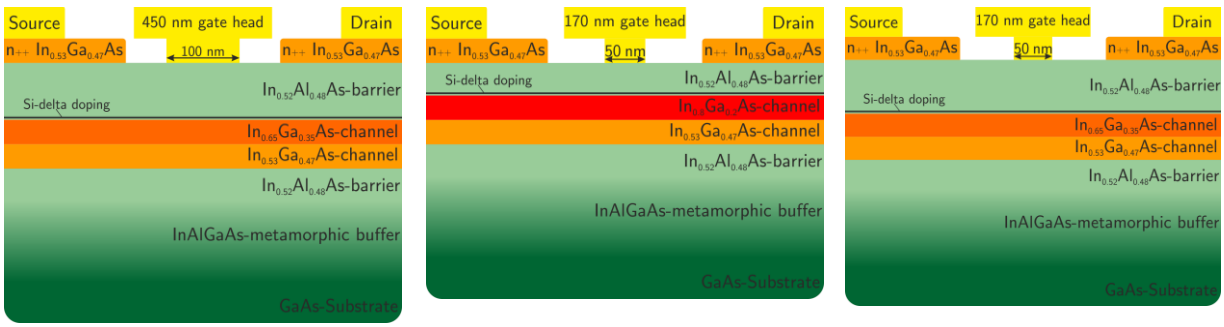
The read-out of quantum bits (qubits) require the noise added by the electronics to be as low as possible to not disturb the extremely weak signals. Typical qubits today operate in the lower gigahertz frequency regime. The transistor technology in which a LNA is built determines the noise performance that can be reached by proper circuit design. Lowest noise performance at room temperature and at cryogenic temperatures have been demonstrated by InGaAs high-electron-mobility transistors (HEMTs), which can be implemented either directly lattice matched on InP-substrate [4.1] or with a metamorphic buffer on GaAs substrate [4.2], [4.3], [4.4], then called metamorphic HEMTs (mHEMTs).

Further reduction of the noise of today's low-noise amplifiers (LNAs) needs the transistor technology to be optimized for cryogenic ultra-low-noise amplification. Historically, the noise performance has been improved by gate length scaling [4.5], which leads to higher gain, transition frequency f_T, and f_{max} [4.6], [4.7] suppressing the high output related channel noise of the HEMTs [8]. However, when scaling below the 100 nm node the improvement fell short of expectations, which has been observed by several groups. The direct comparison of two almost identical LNAs in 50 nm and 35 nm mHEMT revealed a much higher sensitivity of the noise performance of the longer gate length amplifier. This behaviour is unexpected since short channel effects seem to appear at longer gate length.

A comprehensive study that does account for more parameters than just the gate length is mandatory to further improve the noise performance of today's HEMTs. Fraunhofer IAF's mHEMT technologies of with gate length of 100 nm [4.2], 50 nm [4.3], and 35 nm [4.4] are excellent candidates to investigate the impact of different technological parameters on the overall noise performance since they have been developed by subsequent gate length scaling. In addition, two epitaxial variations of the established 50 nm technology (50 nm Technology A) have been processed to investigate the influence of the epitaxial layer stack on the cryogenic noise performance [4.9]. The processing of the wafers is identical to the established version and only the epitaxial layer stack has been adapted.

The first variation (50 nm Technology B) targets to investigate the influence of the InAlAs barrier thickness on the gate-leakage current, which is a source of noise in short gate length HEMTs. The epitaxial structure of the 100 nm mHEMT technology has been used due to its availability and higher barrier layer thickness.

The second variation (50 nmTechnology C) targets to investigate the influence of the channel structure on the noise performance. Instead of a composite channel, as it is used in 100 nm and 50 nm Technology A and B, a single channel with 80% indium content is used without changing other epitaxial properties compared to the established version. Fig. 4.1 compares the different epitaxial layer stacks of the five technologies investigated based on their cross section.



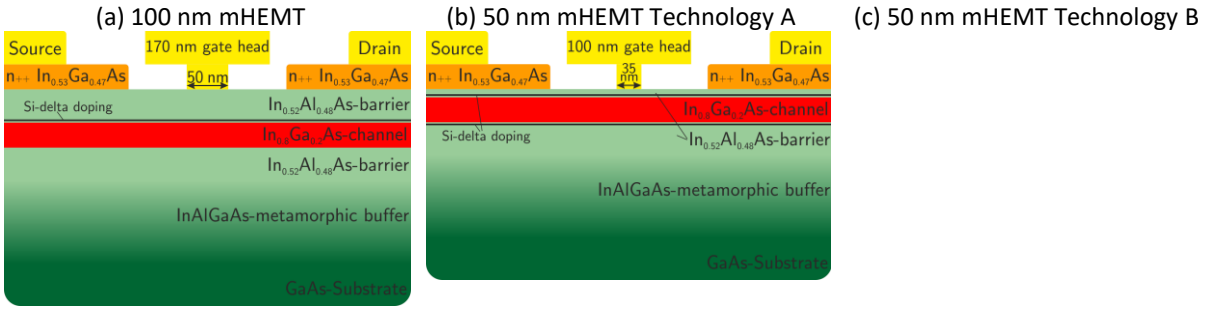
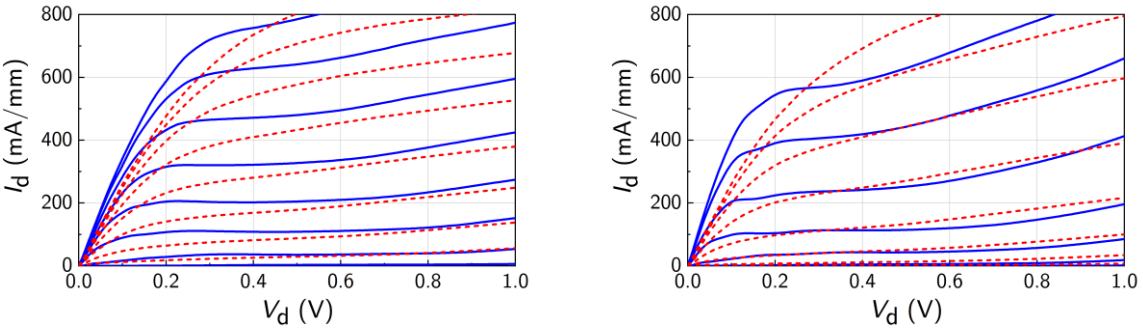


Fig. 4.1. Epitaxial layer stacks of the different mHEMT technologies that have been investigated (representations are not true to scale). (a) 100 nm mHEMT, (b) 50 nm Technology A, (c) 50 nm Technology B, (d) 50 nm Technology C, and 35 nm mHEMT are shown.

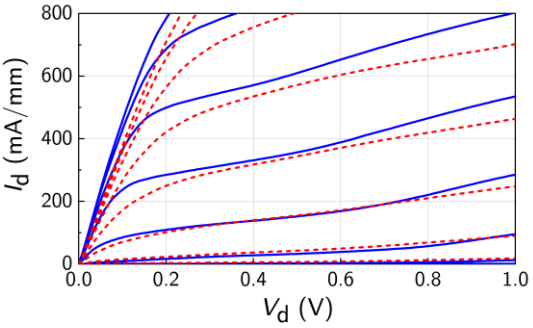
4.2 DC Characterization

The five technologies investigated have been dc characterized both at room and at cryogenic temperature. Fig. 4.2 shows the measured output current-voltage characteristics. The drain voltage has been swept in 25 mV steps and while the gate voltage was varied in 0.1 V steps from -0.2 V to 0.5 V. A kink-free output characteristic is found for all technologies both at cryogenic and room temperature. The transistor on-state resistance improves upon cooling to 10 K for all technologies. This is likely to originate from lower parasitic resistances and higher electron mobility at cryogenic operation.



(a) 100 nm mHEMT (b) 50 nm mHEMT Technology A

(c) 50 nm mHEMT Technology B (d) 50 nm mHEMT Technology C



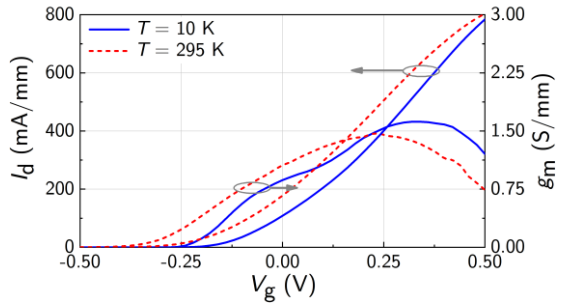
(e) 35 nm mHEMT

Fig. 4.2. Output current-voltage characteristics of 2 × 60 µm mHEMTs measured at 295 K (red, dashed) and 10 K (blue, solid). (a) 100 nm mHEMT, (b) 50 nm Technology A, (c) 50 nm Technology B, (d) 50 nm Technology C, and 35 nm mHEMT are shown.

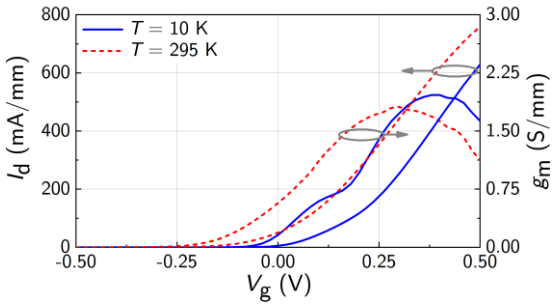
The transfer characteristic of the different technologies has been measured for all technologies investigated both at cryogenic and room temperature. Fig. 4.3 shows the transfer characteristics of 2 × 60 µm HEMTs at a drain voltage of V_d = 0.5 V. The gate-voltage has been swept in 20 mV steps and the drain current is measured. The dc-transconductance is obtained as the discrete derivative of the drain current with respect to the gate voltage.

Common to all technologies is a shift of the threshold voltage at cryogenic temperatures. Furthermore, the peak transconductance increases for all technologies. At room temperature, all technologies show a smooth increase of transconductance with gate voltage. At cryogenic conditions, a plateau can be observed in the transconductance curve of the 100 nm mHEMT, 50 nm mHEMT Technology A, and 50 nm mHEMT Technology B. No plateau is found for 50 nm mHEMT Technology C and 35 nm mHEMT. Therefore, the plateau behaviour seems to be independent of the gate length. It has been found that all technologies that use a composite channel exhibit the plateau at cryogenic temperature. Hence, the change in transconductance seems to originate from the composite channel structure.

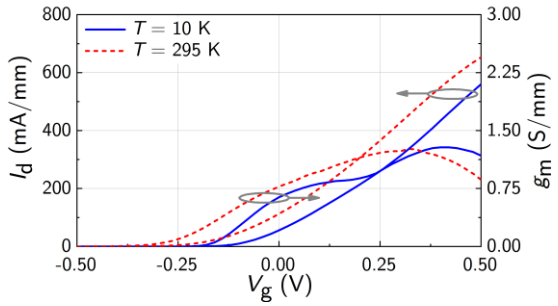
High transconductance at low currents is needed for ultra-low-noise amplification to achieve high gain suppressing the channel noise, which increases with drain current. Therefore, it is of special interest how much transconductance is achieved for a certain drain current. Fig. 4.4 shows the measured transconductance of the different HEMT technologies as a function of the drain current at a temperature of 10 K.



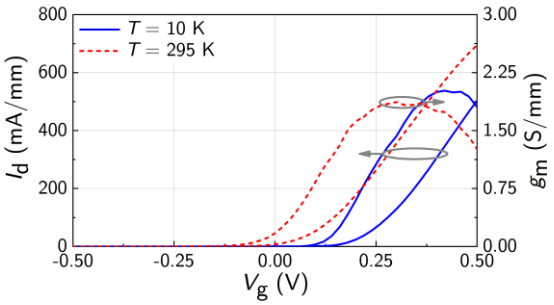
(a) 100 nm mHEMT



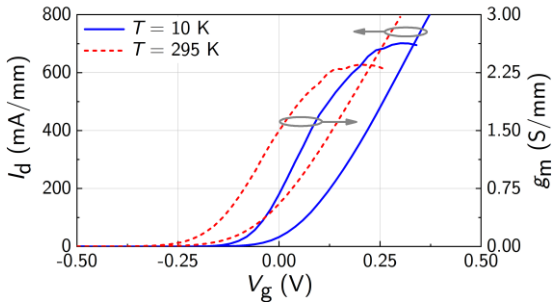
(b) 50 nm Technology A



(c) 50 nm Technology B



(d) 50 nm Technology C



(e) 35 nm mHEMT

Fig. 4.3. DC transfer characteristics of 2 × 60 µm mHEMTs at room (red, dashed) and at cryogenic temperatures (blue, solid) at a drain voltage of V_d = 0.5 V. (a) 100 nm mHEMT, (b) 50 nm Technology A, (c) 50 nm Technology B, (d) 50 nm Technology C, and 35 nm mHEMT are shown.

In Fig. 4.4, it can be seen that the plateau shifts high transconductance values toward high drain currents, which is disadvantageous for low noise operation since the same amount of gain is achieved at the cost of higher channel noise power.

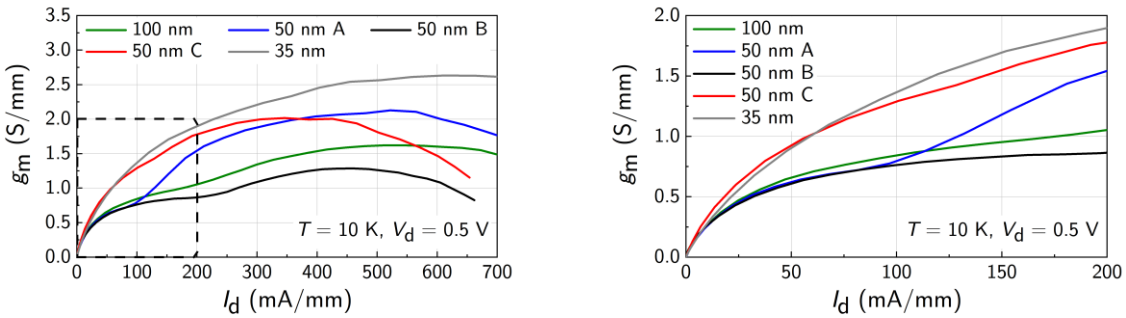


Fig. 4.4. DC transconductance measurements of the different 2 × 60 µm mHEMTs as a function of drain current at 10 K. (Left) full measurement range and (right) close-up view on low noise bias points is shown.

The technologies with a single channel with high indium content show no plateau and therefore, a very steep increase of transconductance with drain current is achieved. The highest peak transconductance is achieved by 35 nm mHEMT at high drain currents. However, 50 nm Technology C shows slightly higher transconductance for drain currents lower than 50 mA/mm. The improvement in transconductance of 50 nm Technology C in comparison to the established 50 nm Technology A is mentionable since it is approximately 50% higher at 50 mA/mm. An improvement in noise performance is expected from this since the same amount of gain can be achieved with lower channel noise or higher gain at the same amount of channel noise.

The gate-leakage currents of all technologies have been measured at room temperature and at 10 K since it adds shot noise at the gate of the device and shall be as low as possible. Fig. 4.5 compares the magnitude of the measured gate currents of the different technologies. The magnitude of the gate-leakage current reduces for all technologies when cooled to 10 K by approximately one order of magnitude.

The gate-currents of all technologies besides 35 nm mHEMT are approximately in the same order of magnitude at both temperatures. 35 nm mHEMT shows by approximately two orders of magnitude higher gate-leakage currents. This is likely to be caused by tunnelling of the electrons through the thin InAlAs barrier layer. The barrier of the 35 nm technology is lower compared to the other technologies to allow for proper channel electron control at very short gate length, which leads to high tunnelling. Since tunnelling is to the greatest extent temperature independent, high leakage is observed at both temperatures. The lowest leakage currents are observed for 50 nm Technology B, which has an increased barrier height to decrease gate leakage. This however comes at the cost of decreased channel control (much lower transconductance, see in Fig. 4.4 and Fig. 4.3).

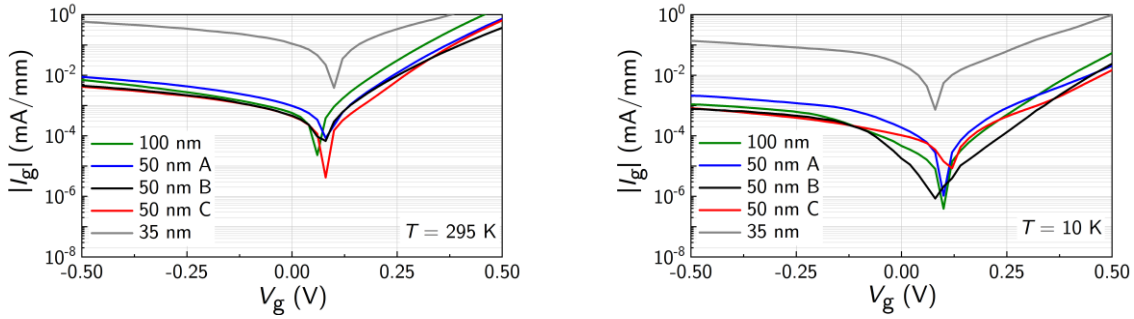


Fig. 4.5. Gate-leakage current measurements at room (left) and cryogenic (right) temperatures of the different mHEMT technologies at a drain voltage of 0.5 V.

4.3 RF-Characterization

Cryogenic on-chip S-parameters up to 50 GHz have been measured at 10 K of all technologies investigated. The transition frequency f_T is a widely used figure of merit for RF current gain and is the main channel noise suppression factor in Pospieszalski's [4.8] and Fukui's [4.10] relation for the minimum noise temperature of a transistor.

f_T has been extrapolated from the S-parameter measurements by calculating h_{21} from the measurements and fitting a line (logarithmic scale) with fixed slope of -20 dB/decade to the measured h_{21}. The zero-crossing provides f_T (see Fig. 4.6 (f)). Fig. 4.6 shows f_T of 2 × 60 µm HEMTs of the different technologies investigated as a function of drain current and voltage. The circles denote the bias points at which S-parameters have been measured and the contour is obtained by interpolation between these bias points.

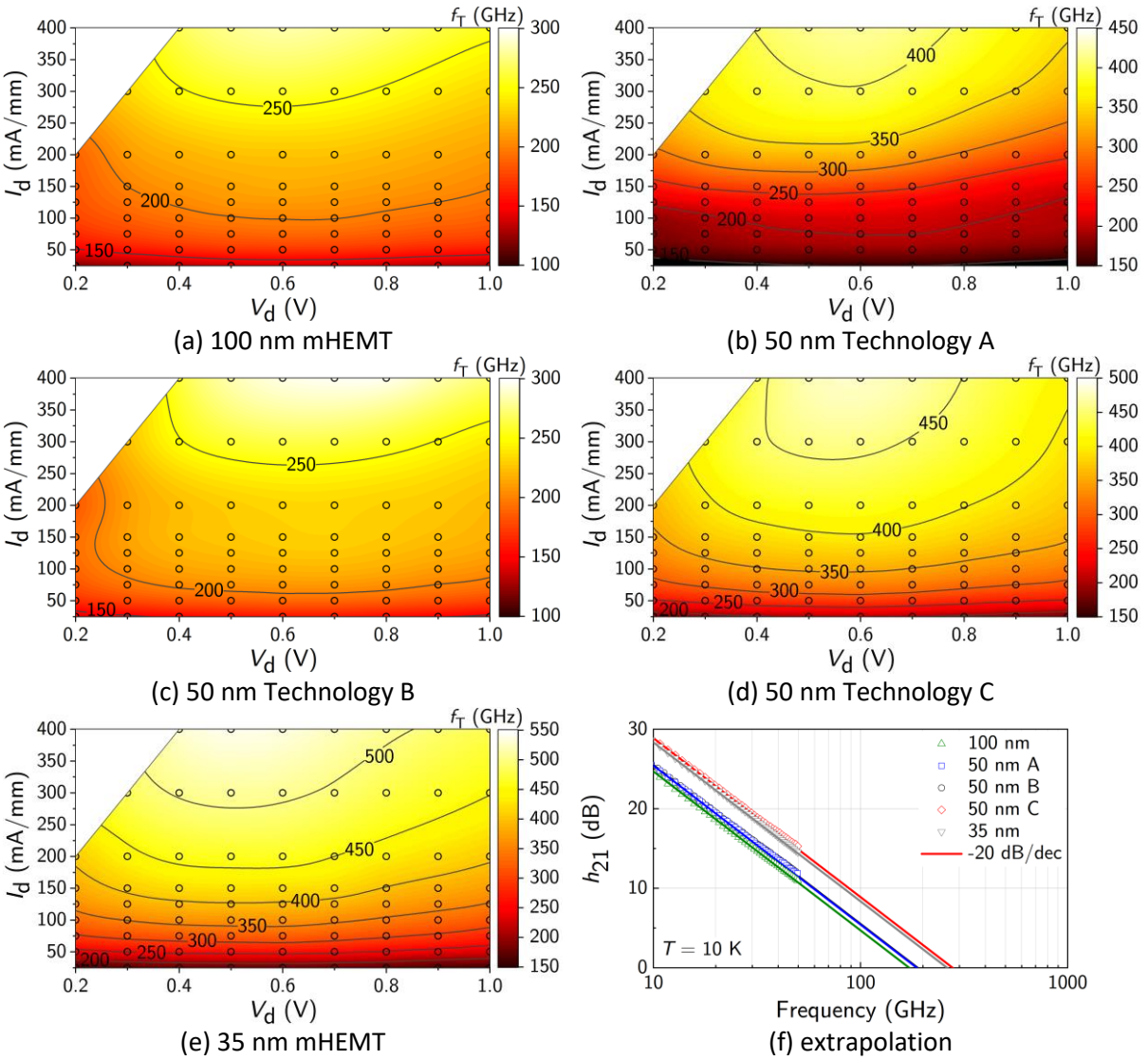


Fig. 4.6. f_T as a function of the drain voltage and drain current extrapolated from S-parameter measurements of 2 × 60 µm up to 50 GHz operated at 10 K. (a) 100 nm mHEMT, (b) 50 nm Technology A, (c) 50 nm Technology B, (d) 50 nm Technology C, and 35 nm mHEMT are shown. (f) shows the extrapolation at V_d = 0.5 V and I_d = 50 mA/mm. Circles denote the bias points at which S-parameters have been measured and the contour is obtained by interpolation between these.

The 100 nm mHEMT technology has the lowest f_T value over the complete bias range which has been expected due to the long gate length. However, 50 nm Technology B shows only a minor improvement over 100 nm mHEMT, which matches the observed dc characteristics (low transconductance). The gate barrier of variation B is not optimized for a 50 nm gate, which reduces the channel control and the f_T improvement due to a shorter gate length is small. The 50 nm Technology A has a by over 100 GHz higher peak f_T compared to variation B and 100 nm mHEMT. However, the increase of f_T with the drain current is low at small drain currents. In the lower bias regime, Technology A only yields a minor improvement in comparison to 100 nm mHEMT and Technology B. The 50 nm technology variation C and the 35 nm technology both show a very high increase of f_T with increasing drain current. The maximum f_T of 50 nm Technology C is over 75 GHz higher compared to Technology A and especially the improvement at low currents is impressive since the improvement of approximately 75 GHz is already achieved at a drain current of only 50 mA/mm. As expected, the 35 nm

mHEMT has the highest f_T at high drain currents. Nevertheless, the f_T performance below 125 mA/mm is approximately equal to 50 nm Technology C.

The measured f_T performance matches the findings from the DC characterization. Furthermore, it is ensured that no large capacitances are introduced for the promising 50 nm single channel Technology C, which would have reduced f_T and has not been observed.

4.4 RF Noise Characterization

The RF noise performance of the different technologies has been investigated using a three stage extended Ku-band (12 – 18 GHz) LNA MMIC that has been processed in the different technologies to allow for highest comparability. A 35 nm MMIC has not been processed since an increased noise temperature is to be expected in the Ku-band due to the increased leakage current. Fig. 4.7 shows a chip micrograph of the three stage LNA MMIC and Fig. 4.8 shows the corresponding simplified schematic. LNAs need to be used to measure the noise temperature under cryogenic conditions since single transistor devices are highly mismatched and have not enough gain to achieve proper RF noise measurements.

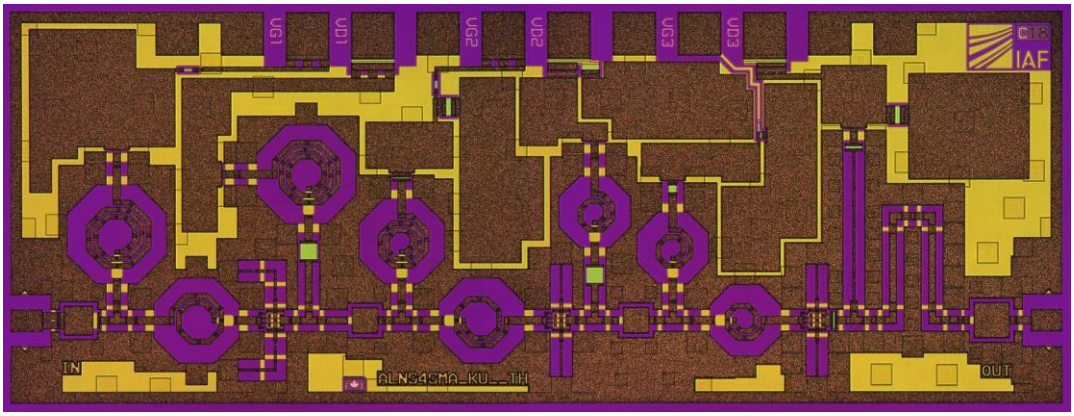


Fig. 4.7. Chip micrograph of a 3-stage Ku-band LNA. The chip occupies an area of 2.5 × 1 mm^2.

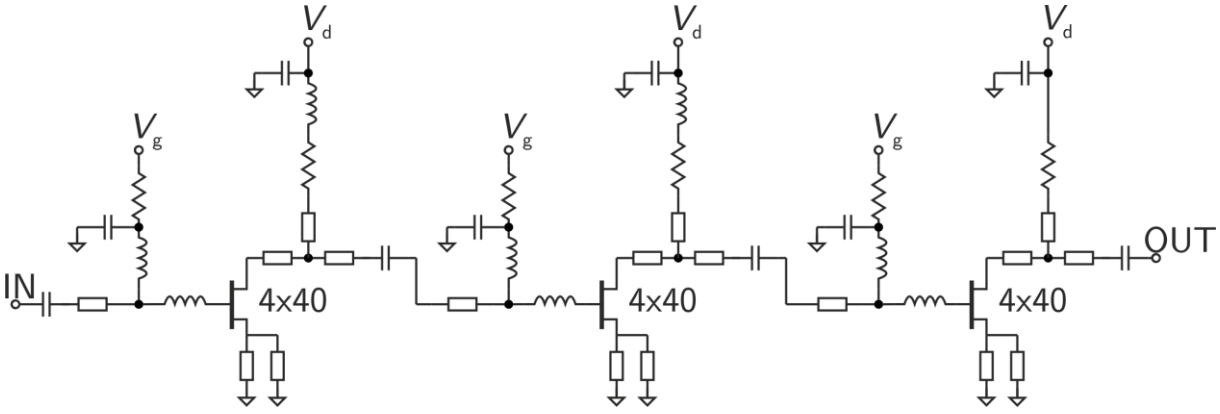


Fig. 4.8. Simplified schematic of the three stage Ku-band LNA.

At first, the room temperature performance of the four LNA MMICs has been investigated. Room temperature noise temperature measurements are performed using a Keysight PNA-X vector network analyzer with a highly sensitive receiver dedicated to noise measurements and an input tuner that allows for vector corrected noise measurements. S-parameters and noise are measured in one

probe contact using the cold-source method [4.11]. Fig. 4.9 shows the room temperature small-signal gain and the corresponding noise temperature measurements of the Ku-band LNAs in the four different technologies.

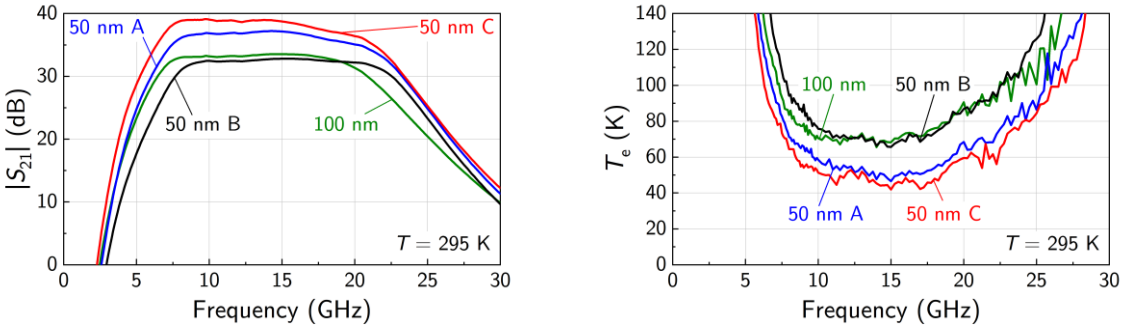


Fig. 4.9. Room temperature small-signal gain (left) and noise temperature measurement of the Ku-band LNAs in the different technologies.

The Ku-band LNA in 100 nm technology and the 50 nm Technology B exhibit the lowest gain at room temperature of 33.2 dB and 32.3 dB (on average), respectively. Variation A has a higher average gain of 36.4 dB over the amplifier bandwidth and Technology C has the highest average gain of the four technologies with 38.7 dB. The noise temperature is highest for the 50 nm Technology B with 76.3K between 8 and 18 GHz. However, the 100 nm technology shows only a slightly improved noise temperature of 73.2 K. The noise temperature decreases significantly for 50 nm Technology A, which provides on average 57.7K of effective input noise temperature. The lowest noise temperature is observed for 50 nm Technology C, with only 51 K average noise temperature from 8 – 18 GHz and a minimum of only 41.9 K.

Cryogenic on-chip noise temperature measurements have been performed using the cold attenuator method [4.12]. A previously characterized 20 dB attenuator MMIC with integrated temperature sensor is glued in front of the device under test (DUT) and electrical connections are implemented via wire bonding. The Y-factor method is used to calculate the noise temperature and the cold and hot state is provided by a Keysight 346C noise diode. The resulting output noise powers are measured using an Agilent N8975A noise figure analyser (NFA). The worst-case uncertainty of the measurement setup has been estimated to be ±1.4 K accounting for the diode ENR uncertainty, the uncertainty of the attenuator temperature sensor, probe arm noise temperature uncertainty, NFA measurement uncertainty, and mismatch of all components in the measurement chain.

Fig. 4.10 shows the measured scalar gain and noise temperature of the Ku-band LNAs of the various technologies considered at 10 K. The LNAs are operated at the bias point where the noise temperature of the respective technology becomes minimal.

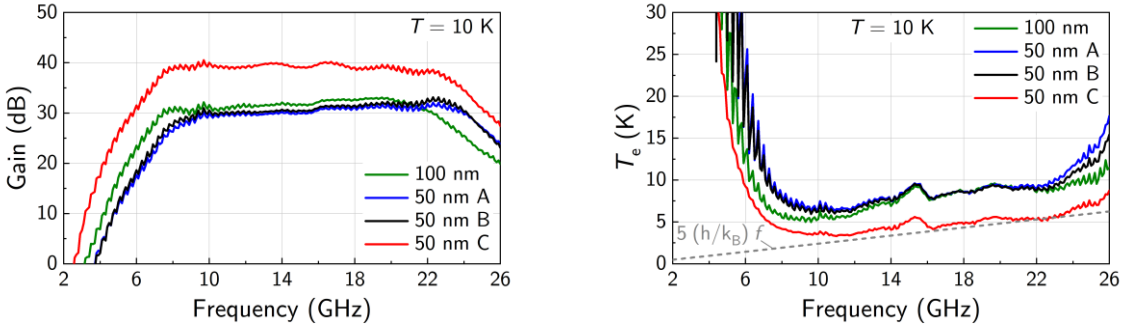


Fig. 4.10. Scalar gain (left) and noise temperature (right) measurements of the Ku-band LNAs in dif-

ferent technologies at 10 K.

At cryogenic temperatures, the 100 nm mHEMT technology exhibits an average gain of 31.5 dB from 8–18 GHz. The gain of the 50 nm mHEMT Technology A and B is almost identical in the chosen bias point with average values of 29.7 and 30.3 dB between 8 and 18 GHz, respectively. A significant improvement in gain is observed for 50 nm Technology C (as it is observed at room temperature as well), which shows an average gain of 39.4 dB between 8–18 GHz with a maximum value of 40.5 dB.

The highest noise temperature at 10 K has been measured for 50 nm Technology A and B, which are almost identical and yield on average 7.6 K and 7.5 K noise temperature, respectively. The 100 nm mHEMT shows a slightly lower average noise temperature of 6.9 K. The 50 nm Technology C exhibits the lowest noise temperature with only 4.2K on average between 8 and 18 GHz with a minimum of 3.3 K at 11 GHz at an ambient temperature of 10 K.

The cryogenic LNA performance is in good agreement with the DC and RF data of single HEMTs at cryogenic conditions. Higher transconductance values translate to higher amplifier gain. Especially the high transconductance at very low drain currents of 50 nm Technology C boost the performance at cryogenic conditions. High gain (more than 39 dB on average) at very low channel noise power due to low drain currents lead to very low amplifier noise temperatures. The high transconductance of the 50 nm Technology C has been achieved by the usage of a single channel with high indium content. Furthermore, a InAlAs barrier that is thick enough to allow only small gate-leakage currents to flow, but thin enough to allow for proper channel control at 50 nm gate length for high transconductance is important for ultra-low-noise amplification.

Compared to Ku-band LNAs in the literature, the Ku-band LNA in 50 nm Technology C sets the state of the art with its average noise temperature of 4.2 K between 8 and 18 GHz [4.9].

5 RF characterization of III-V nanowires (Contributor: ULUND)

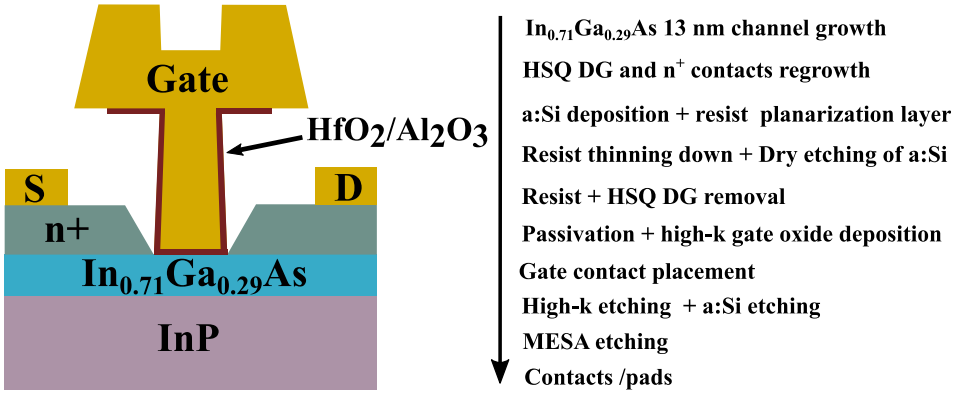
Roadmaps in device technology have predicted a switch from planar channels and fins in silicon to 3D stacked gate-all-around nanowires in III-V technology. Along this line, IBM recently unveiled a new 2 nm technology node (https://www.anandtech.com/show/16656/ibm-creates-first-2nm-chip) that use three-stack gate-all-around nanosheets in silicon. The work at ULUND focuses on III-V nanowire MOSFET technology in lateral and vertical channels, as well as III-V nanowire TFETs in vertical channels. Nanowires are selectively grown on the substrate, either silicon or III-V via a buffer layer. Nanowire growth in the vertical direction allows mitigation of the lattice constant mismatch in heterostructures and allows improved crystal quality.

5.1 Introduction

ULUND presents data from three different III-V device technologies: planar (a test vehicle for lateral nanowire) MOSFETs [5.1-5.2], vertical nanowire MOSFETs [5.3-5.5], and vertical nanowire TFETs [5.6-5.7]. These three device technologies share many features, such non-planar gates on III-V channel and high-k gate oxides. This gives a potential for very high gm and low Ron. However, each has their own strengths that gives additional specific performance advantages. The lateral nanowire MOSFETs provide regrown contacts in a HEMT-like structure. The vertical MOSFETs provide true gate-all-around electrostatics and routing on different levels. The vertical TFETs also change the physics in the channel to allow sub-thermionic switching behavior.

These device technologies are tested in DC IV (transfer characteristics, output characteristics), RF scattering parameters (S-parameters-freq, fT, fmax, Y-parameters vs freq, gm-freq and gd-freq dispersion), and pulsed IV (transfer characteristics, output characteristics, and modified Id-time step response). The DC and pulsed IV parametric tests are performed at both RT and 12 K. The focus of this deliverable chapter is to demonstrate measured cryogenic test results and presenting dynamic effects due to gate oxide traps and self-heating effects in the III-V nanowire MOSFETs/ TFETs.

A planar InGaAs-based quantum well MOSFET with regrown contacts are fabricated, aiming for millimetre wave applications. This device drives a substantial technology development from earlier device generations [5.1] and serves as a test vehicle for lateral nanowire MOSFETs [5.2]. A lateral nanowire device can be formed in the same process flow by masking the In-rich pseudo-morphic channel growth. The frequency/time domain analyses are done and expect similar results for lateral nanowire transistor except with better electrostatics. The device cross section schematic is shown in Fig. 5.1 along with the main fabrication steps.



(a) (b)

Fig. 5.1. (a) Schematic view of the planar $In_{0.71}Ga_{0.29}As$ MOSFET (b) along with a description of the main fabrication steps used to form the device structure.

The fabrication process for the vertical InGaAs nanowire MOSFET is based on VLS epitaxial growth and processing in the vertical direction [5.4-5.5]. First, i-InAs wire segments are grown, using Au seed particles, from an InAs buffer layer on Si substrate. Gradually Ga precursors are introduced in the reactor to form a highly doped InGaAs on the top, which acts as the drain terminal for the device. The transistor has a 50 nm thick HSQ first spacer, a 5 nm thick Al2O3/HfO2 bilayer gate oxide, and a 60 nm thick W gate. S1800 resist forms the second spacer. The device cross section schematic is shown in Fig. 5.2.

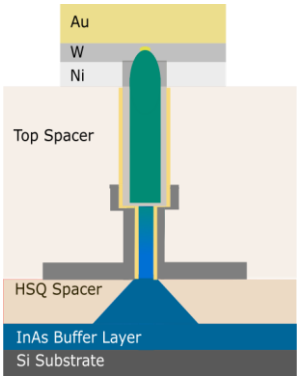
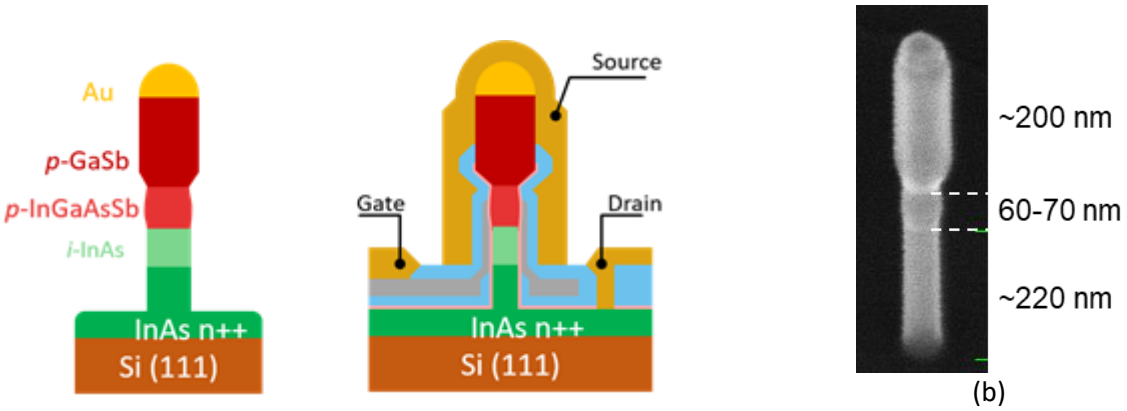


Fig. 5.2. Schematic view of a vertical InGaAs nanowire MOSFETs on Si substrate.

The fabrication process for vertical nanowire TFET starts similar to the nanowire MOSFET, but utilises another III-V heterostructure [5.6-5.7]. First, n-doped InAs is grown on Si substrate, on which Au seed particles are deposited. The vertical nanowires consist of segments with composition of i-InAs/ p+ GaAs0.72Sb0.28 /p+ GaSb that are grown using the Vapor Liquid Solid (VLS) method. A trilayer of high-k stack consisting of 1nm Al2O3/ 3 nm HfO2/ 10 nm Al2O3 is deposited with ALD, of which, 1nm Al2O3/3 nm HfO2 with EOT of 1 nm forms the gate oxide. The tunnel junction of i-InAs – p+ GaAsSb is gated with W of 30 nm thickness. The spacer between source, gate and drain are the trilayer and 10 nm Al2O3 layer respectively. The device cross section schematic is shown in Fig. 5.3, before and after device processing, along with an electron micrograph of the grown wire prior to device processing.



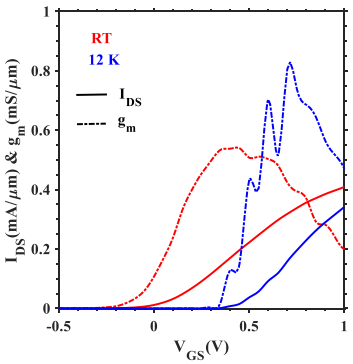
(a) (b)

Fig. 5.3. (a) Schematic view of a vertical InGaAsSb nanowire TFETs on Si substrate and (b) also showing an electron micrograph of the nanowire before device processing.

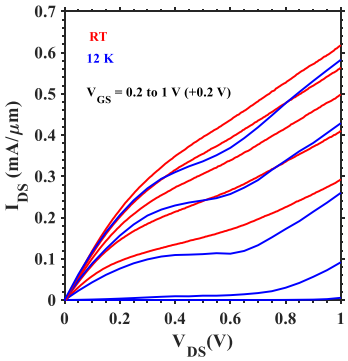
5.2 DC characterization of nanowire MOSFETs at RT and 12 K

The DC measurements are performed using a semiconductor parameter analyzer with Kelvin triax connections to the probe needle. This highlights the basic characteristics of the different nanowire technologies and provides a baseline for the RF and pulsed IV tests presented below.

The planar InGaAs MOSFETs transfer and output characteristics in Fig. 5.4 shows improvement in gm (35% increase) and higher VT at 12 K. The inverse sub threshold swing of the device at 150 mV/dec at RT and 50 mV/dec at 12 K. Observed Ron are about 1.6 kΩμm and 1.3 kΩμm, respectively, at RT and 12K, for gate overdrive voltage of 0.3 V.



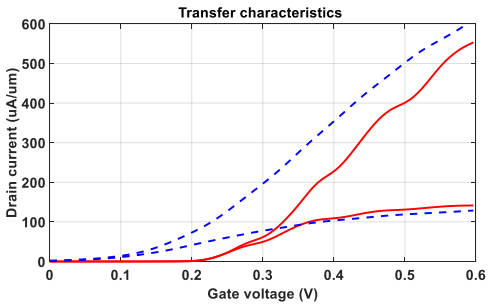
(a)



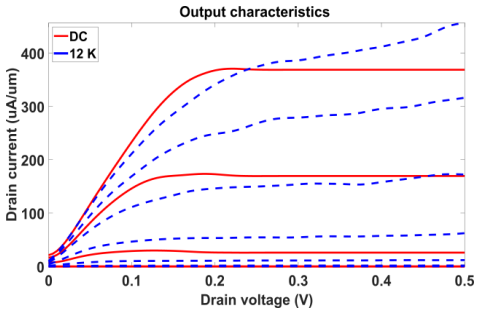
(b)

Fig. 5.4. (a) The transfer and (b) output characteristics of the device with L_g = 60 nm, W_g = 20 µm at room temperature (red) and at 12 K (blue).

The vertical InGaAs nanowire MOSFET transfer and output characteristics in Fig. 5.5 show increased VT at 12 K, compared to RT. Data at 12 K also show visible steps in the transfer, what we attribute to quantization, and a negligible output conductance. The reduced output conductance can in part indicate self-heating, but is also in part expected from a thermal injection perspective with efficient electrostatics in a nanowire channel.



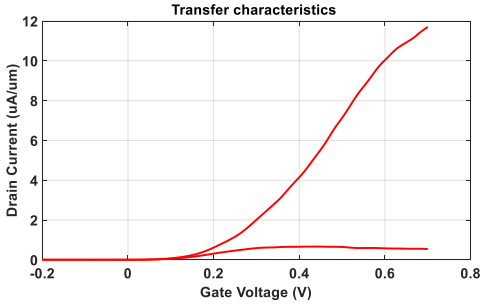
(a)



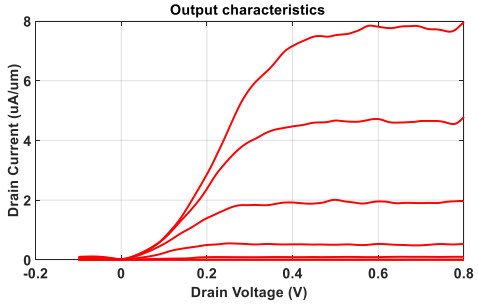
(b)

Fig. 5.5. Transfer and output characteristics of a vertical nanowire MOSFET – RT (blue dash) and 12 K (red line). The transistor has 70 nm gate length, diameter of 28 nm. Number of nanowires is 1.

The vertical InGaAsSb nanowire TFET transfer and output characteristics at RT are shown in Fig. 5.6 for reference. It is included here for completeness but will not be analyzed further in this report.



(a)



(b)

Fig. 5.6. Transfer and output characteristics of a vertical nanowire TFET at RT. The transistor has gate length of 220 nm, diameter of 22 nm. Number of nanowires is 1.

5.3 RF characterization of lateral nanowire MOSFETs at RT

The RF measurements are performed at RT with a R&S ZVA67 vector network analyser (VNA) sweeping 10 MHz-67 GHz using -27 dBm channel power and 20 Hz IF bandwidth. The VNA is off-chip calibrated to the probe tips. The measurements are also on-chip deembedded using a two-step method (open-short) prior to analysis of the cutoff frequency and details of the device parameters, as previously demonstrated on lateral and vertical devices [5.8-5.10].

The scattering parameters of the planar InGaAs MOSFET are shown in Fig. 5.7. The device exhibits peak f_T/f_{max} of 194/161 GHz at V_{GS} = 0.25 V, V_{DS} = 1 V with MSG of 14 dB at 20 GHz.

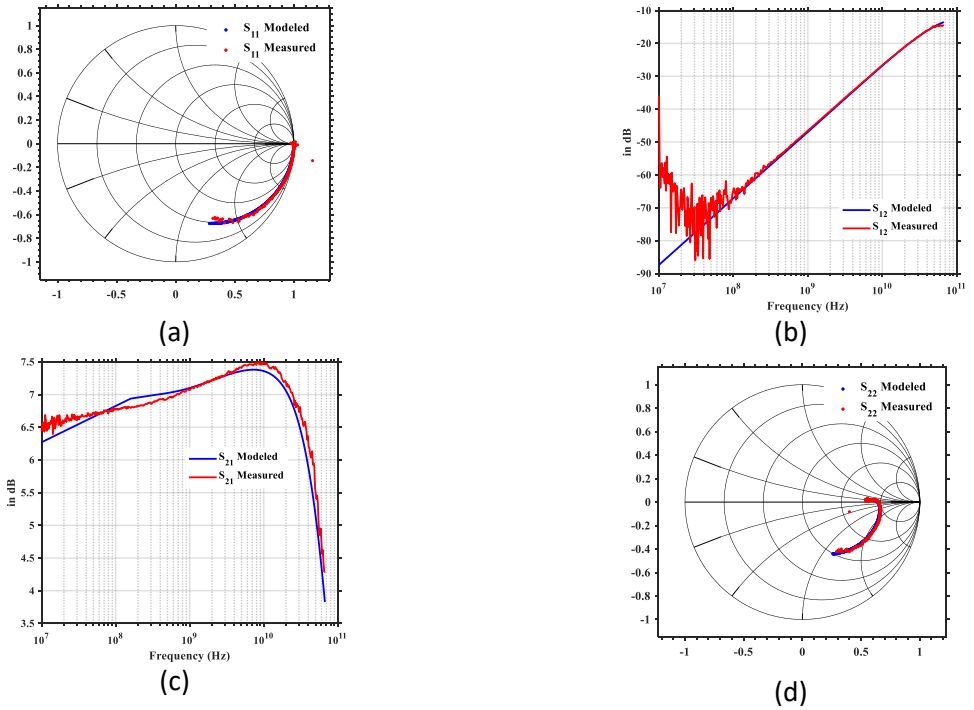


Fig. 5.7. Scattering parameters of the planar InGaAs MOSFET with L_g=60nm and W_g=20µm measured at V_{GS}=0.25V and V_{DS}=1V.

Intrinsic Y-parameters are shown in Fig. 5.8, after removing extrinsic pad/contacts capacitances and resistances. Logarithmic frequency dispersion in real(Y_{21}) is observed which is attributed to border traps in the high-k gate oxide. Ideally, we should observe similar logarithmic frequency dispersion in real(Y_{22}), however impact ionization is dominant. The same can be explained for inductive behavior in S_{22}. Here to obtain a good fit to real(Y_{22}), impact ionization/band to band tunneling current sources are modeled as sum of three different independent sources.

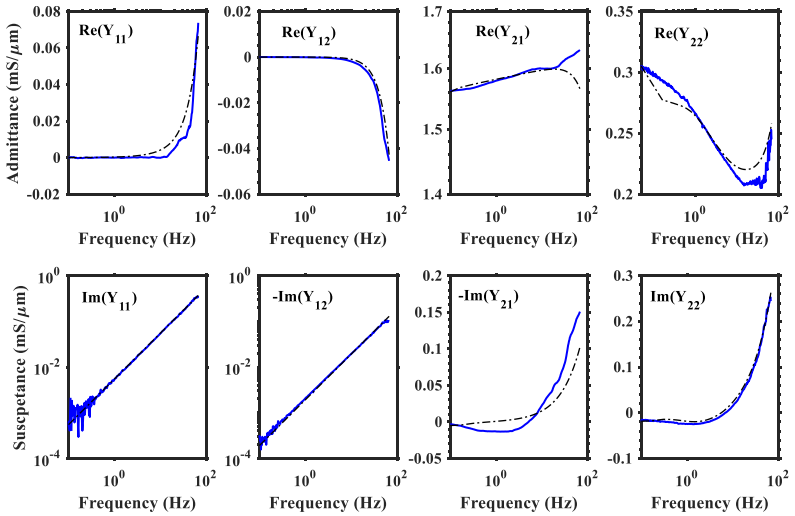


Fig. 5.8. The Y parameters of the device with L_g=60nm, W_g=20µm at V_{GS}=0.25V, V_{DS}=1V.

The small signal model used to model the admittance response is shown in Fig. 5.9. Analysis of the admittance parameters, derived from scattering parameters, reveals details of the device characteristics that can be connected to the physical structure and materials in the device. It is especially interesting to look at the frequency dispersion of the transconductance, gm, and output conductance, gd. The former can reveal effects from border traps [5.9] and the latter effects due to self-heating of the device [5.11-5.15]. Border traps distributed in the gate oxide will yield a logarithmic response, a linear increase of gm versus exponential increase of frequency, $g_m \propto g_{m,i}[1 - \ln(\omega/\omega_0)]$ where $\omega < \omega_0$. This yields from a distribution of time-constants, describing tunnelling into and out of the border traps at different oxide depth. Self-heating effects can be seen in similar transitions of the output conductance, but primarily at specific time constants, based on thermal transport dynamics in the device. Note that scattering / AC evaluation, performed at a bias point, does not reveal non-heated characteristics of the device. The self-heating transition in gd corresponds to the shift from periodically heated to isothermal response.

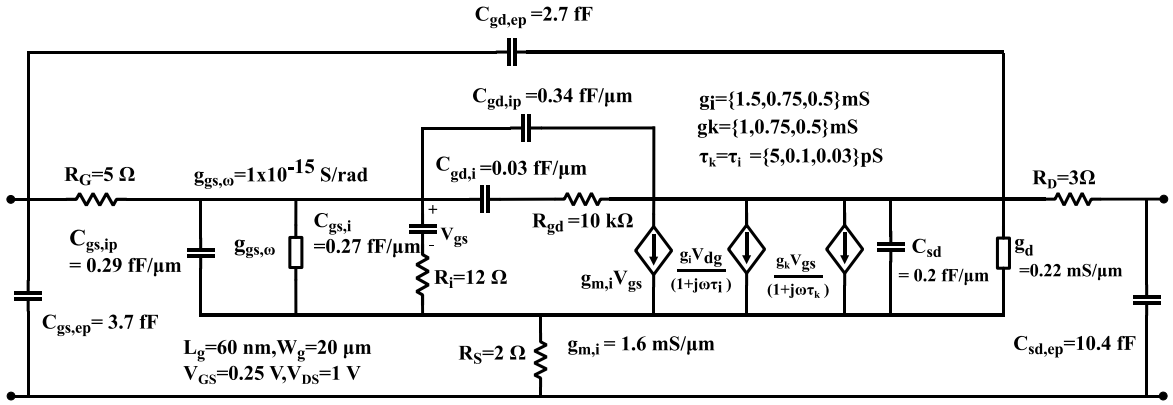
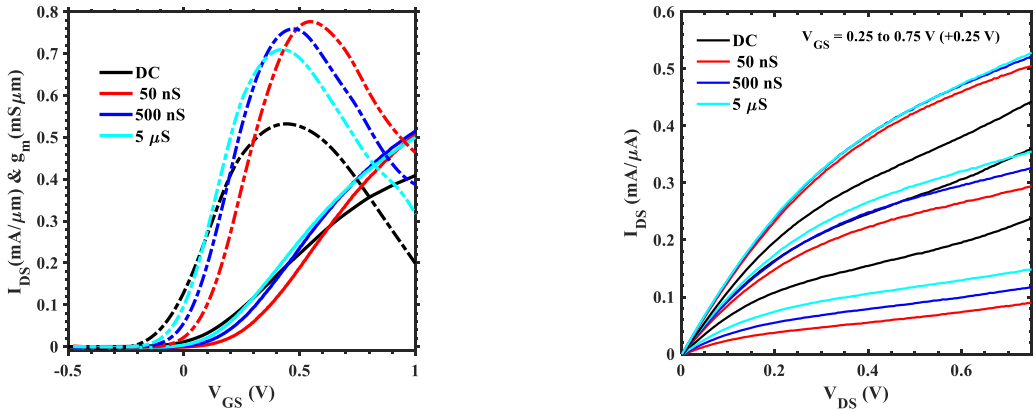


Fig. 5.9. The small signal model used to model the intrinsic Y-parameters and gains of the device with L_g = 60 nm, W_g = 20 µm. The device has f_T/f_{max} of 194/161 GHz at V_{GS} = 0.25 V, V_{DS} = 1 V.

5.4 Pulsed IV characterization of nanowire MOSFETs at RT and 12 K

Pulsed IV is performed using a set of linear waveform generators and fast measurement units in a semiconductor parameter analyzer. This evaluates the response during pulse excitations to the device terminals. It can probe dynamics and hysteresis effects of the device down to high-ns scale, thereby providing a frequency bandwidth up to low-MHz range.

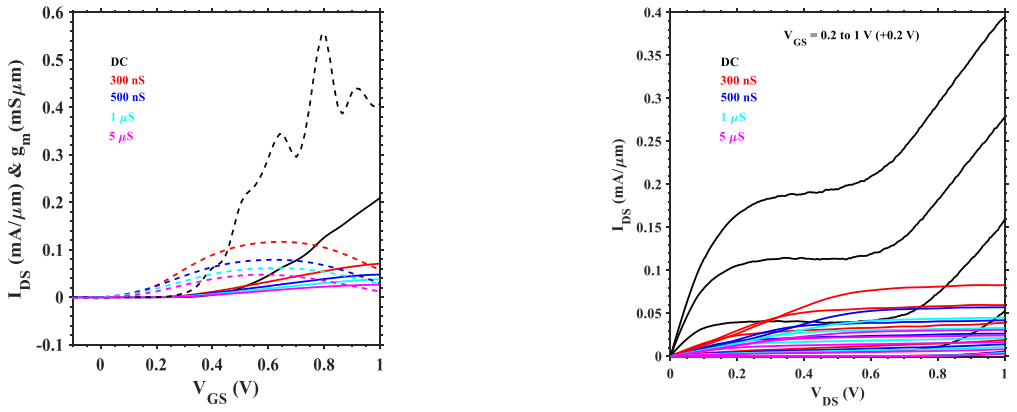
Pulsed IV characteristics for the planar InGaAs MOSFET at RT are shown in Fig. 5.10, compared to DC transfer and output measurements. An increase in g_m, V_T and improvement in SS are observed with reducing pulse width. There is nearly 50% increase in g_m for pulse width of 50 nS. There is no significant change in R_{on} and g_d is observed.



(a) (b)

Fig. 5.10. DC and pulsed IV of a planar InGaAs MOSFET at RT. (a) Transfer characteristics at V_{DS} = 0.5 V and (b) output characteristics of the device with L_g = 60 nm, W_g = 20 µm.

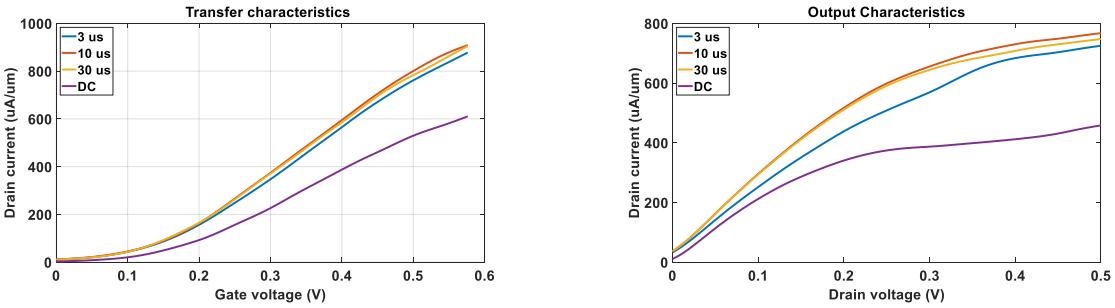
Pulsed IV characteristics for the planar InGaAs MOSFET at 12 K are shown in Fig. 5.11, compared to DC transfer and output measurements. Similar behavior as at RT is observed except that the DC g_m and I_{DS} are higher. Another interesting observation is that DC g_m that is measured after pulsed measurements is lower compared to the DC g_m measured prior to pulsed measurements.



(a) (b)

Fig. 5.11. DC and pulsed IV of a planar InGaAs MOSFET at 12 K. (a) Transfer characteristics at V_{DS} = 0.5 V and (b) output characteristics of the device with L_g = 60 nm, W_g = 20 µm.

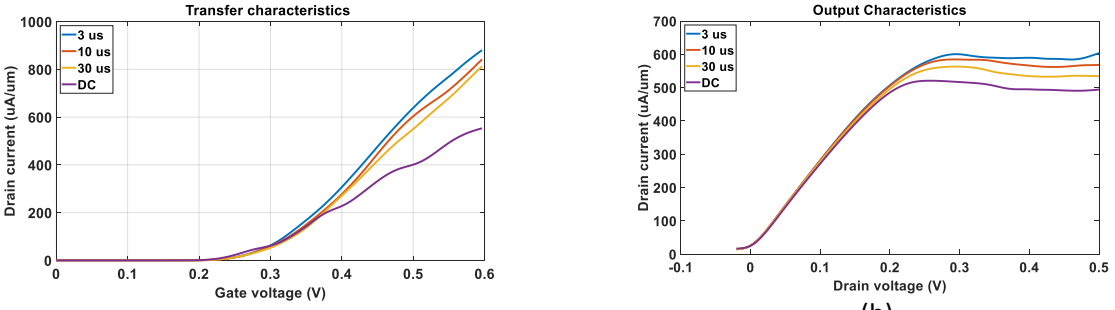
Pulsed IV characteristics for the vertical InGaAs nanowire MOSFET at RT are shown in Fig. 5.12, compared to DC transfer and output measurements. A substantial increase in current is opserved for the pulsed transfer. This is consistent with the theoretical behavior of a MOSFET with border traps in the gate oxide. It is also seen in the output traces that the pulsed IV produces increasingly larger currents responses for shorter pulse lengths.



(a) (b)

Fig. 5.12 DC and pulsed IV of a vertical InGaAs nanowire MOSFET at 12 K. (a) Transfer characteristics at V_{DS} = 0.5 V (b) output characteristics of a single nanowire transistor with gate length of 70 nm, diameter of 28 nm.

Pulsed IV characteristics for the vertical InGaAs nanowire MOSFET at 12 K are shown in Fig. 5.13, compared to DC transfer and output measurements. It is seen that the pulsed IV produces increasingly larger currents responses for shorter pulse lengths. This is consistent with the expected theoretical behavior of a MOSFET with border traps in the gate oxide.



(a) (b)

Fig. 5.13. DC and pulsed IV of a vertical InGaAs nanowire MOSFET at RT. (a) Transfer characteristics at V_{DS} = 0.5 V (b) output characteristics of a single 28 nm diameter nanowire transistor with gate length of 70 nm.

Pulsed IV methods bridge and complement the DC and RF domain methods. It provides another viewpoint of the device characterization compared to traditional steady-state measurements. In relation to DC, it can provide drain current measurements during the onset and action of oxide trap responses and self-heating effects. It is also possible, by custom waveforms and sampling events, to evaluate the gate voltage to drain current step response. This shows effects with similar physical background as frequency dispersion in RF measurements. However, pulsed IV instrumentation allows focus on very low frequency, sub-kHz, characteristics that are not accessible by RF equipment.

The transient step response (modified pulsed IV) show approximately linear drain current decrease in log-log scale, exponential decrease of current in exponential time. This initial exponential decrease versus exponential time is consistent with the gm-f dispersion often observed in RF measurements: linear increase of gm in exponential frequency. We attribute this behaviour to channel charge interaction with border traps in the gate oxide. It can be shown that inelastic tunneling to charge traps uniformly distributed in position and energy would exhibit this response [5.9].

Self-heating effects can also influence the step response of the drain current. This would provide current change related primarily to one dominant time constant, or a set of similar time constants, based on linear heat diffusion in a limited volume. Non-linear effects, for example from temperature dependent material properties, can yield a more complex response. Analysis of self-heating in SOI devices has been performed exhaustively [5.11-5.15], but analysis and modelling in the context of III-V nanowire MOSFETs is yet to be concluded.

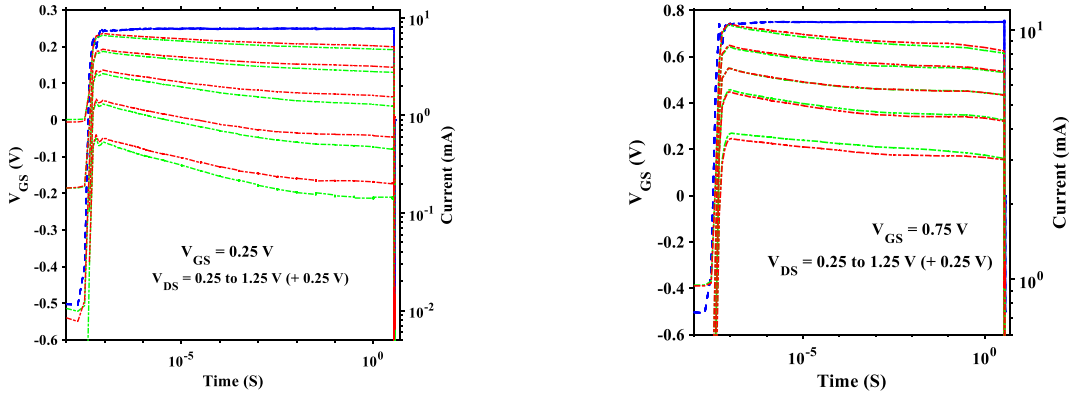


Fig. 5.14. Two successive transient I_{DS} vs V_{GS} (green dot-dash line followed by red dot-dash lines) for various V_{DS} of the device with L_g = 60 nm, W_g = 10 µm at (a) V_{GS} = 0.25 V, (b) V_{GS} = 0.75 V.

6 Summary and conclusions

The Tyndall results show that interactions between oxide defects and free carriers in the semiconductor involve multiphonon transitions; oxide defects at energies aligned with semiconductor bandgap do contribute to the small signal ac response of the MOS structure. The nonlocal model based on NMP theory was used to predict the MOScaps impedance and demonstrates that the interaction between free carriers and oxide defects (either at the interface or in the oxide) is via an inelastic tunneling process and the distinction between ITs and OTs simply relates to the distance from semiconductor/oxide interface. When OTs aligned to the semiconductor bandgap are included, the simulated response of the C-V with frequency can accurately reproduce the experimental characteristics. The impedance measurements at 10K confirm the inelastic tunneling capture and emission of carriers by OTs. The C-V hysteresis results at 10K are unexpected and future work will focus on understanding this behaviour. In the next phase of SEQUENCE, simulation of impedance at cryogenic temperature will be performed to test the defect model developed at room temperature.

The results obtained by LETI and INPG clearly indicate that FDSOI is a good option for cryogenic-CMOS applications. While MOS performance significantly improves with T lowering, reaching $I_{on} >$ 1. 2 mA/μm and f_T close to 500 GHz, high back biasing efficiency remains a powerful tool for circuit optimization down to 4.2 K. Back biasing can be safely used for V_{TH} tunability, improving circuits performance at low T, especially when low dynamic power consumption and high bandwidth are required, for example, in quantum integrated circuits. The g_m/I_{DS} improvement was correlated with

the normalized drain current power spectral density increase at cryogenic T, being the CNF + CMF model valid from 300 down to 4.2 K. Both noise parameters S_{Vfb} and Ω were found to be approximately constant with T, for the studied drain current range. Moreover, the LF noise was found to be almost independent on back bias down to 77K.

Fraunhofer IAF provided a comprehensive study on how different gate length and epitaxial layer stacks affect the cryogenic noise performance of metamorphic HEMTs. HEMTs with 100 nm, 50 nm, and 35 nm gate length, as well as two epitaxial variations of the 50 nm process have been investigated at 295 K and 10 K. The results obtained by Fraunhofer IAF show that the cryogenic noise performance of metamorphic HEMTs with 50 nm gate length can be improved significantly by the use of a precisely scaled InAlAs Schottky barrier layer in combination with a thin InGaAs channel with high indium content. The combination allows for extremely low gate leakage in combination with high transconductance and f_T at very low drain current bias. The high transconductance at low drain currents is achieved by the single channel, which removes a plateau from the transconductance curve that is observed for composite channels. High gain at low channel noise power can be achieved in this way. A Ku-band amplifier in the new 50 nm technology variation C utilizing the before mentioned epitaxial optimizations presents state-of-the-art cryogenic noise performance with 4.2 K average noise temperature between 8 and 18 GHz at an ambient temperature of 10 K. The three stage LNA in 50 nm Technology C exhibits more than 39 dB gain at 10 K.

The results from ULUND indicate that III-V nanowire devices can enjoy performance enhancements under cryogenic operation, as compared to RT. The data set shown here also reveals that there are many hurdles that must be overcome to reliably identify and model the physical origin. Quantization with individual responses of separate sub-bands are seen. Effects due to interface dielectric trap interaction with the channel charge are also demonstrated. This phenomenon yields frequency dispersion in the Y-parameters derived from RF S-parameter measurements. Self-heating, impact ionisation and band-to-band tunnelling also influences the results. Pulsed IV and transient step response of the device (modified pulsed IV) is used to verify the dispersion effects from border traps and self-heating found in DC and frequency domain (S-parameter/ AC), but from the view of the time domain. Further work must be done to quantify and model these effects.

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