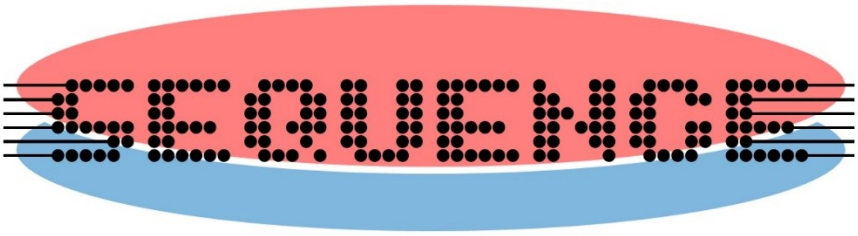
Deliverable – D2.1

First report on electrical characterization and parameter extraction of devices operated at cryogenic condition



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1 Introduction

The objectives of WP2 are i) to perform a detailed LF and RF electrical characterization and parameter extraction of the device operated under deep cryogenic conditions, and, ii) to develop associated LF and RF analytical compact device models valid at very low temperature and usable in circuit design simulation platforms. More specifically, Task 2 and Task 4 of WP2 aim at providing i) basic electrical characterization and improved parameter extraction, ii) insights into carrier transport properties (mobility, velocity) at very low temperature under degenerate statistics conditions for various devices (Si vs III-V) and iii) DC and RF electrical characterization of device operation at extremely low temperatures (20mK-4K) for physical understanding of device operation under deep cryogenic conditions for various Si and III-V devices.

The deliverable D2.1 due at M9 reports on first electrical characterization and parameter extraction carried out on 28nm Si FDSOI devices from industrial platform and on NW, TFET and lateral III-V devices from WP1 consortium.

2 Electrical characterization of FDSOI devices (contributors: LETI, INPG)

2.1 Device under test

The measurements were performed on 28nm FDSOI MOSFETs with t_{si}=7nm and t_{BOX}= 25nm from STMicroelectronics. NMOS and PMOS transistors were processed from (100) handle substrate, with <100>-oriented channel, and HKMG Gate-First architecture (Fig. 2.1) [2.1]. Regular-V_{TH} (RVT) and low-V_{TH} (LVT) transistors are available through a doped back plane (NWELL or PWELL, with typically $N_{A,D}$=10^{18}cm^{-3}) below the BOX. Thin (GO1, EOT=1.1nm) and thick oxide (GO2, EOT=3.2nm) devices have been characterized using a cryogenic prober down to 4.2K.

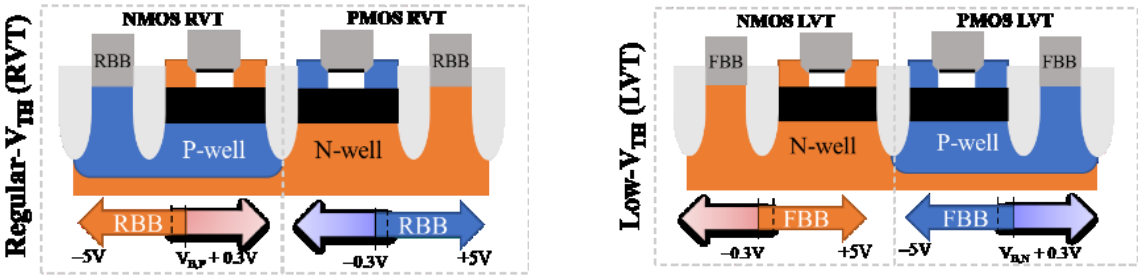


Fig. 2.1. *Schematics of 28nm FDSOI N- and PMOSFETs with regular-V_{TH} (RVT) and low-V_{TH} (LVT) flavors.*

2.2 Capacitance and Charge control

The electrostatic charge control of such FDSOI devices has been characterized by split C-V measurements with a conventional LCR meter. To this end, the gate-to-channel capacitance Cgc=dQi/dVg, has been measured at 1MHz frequency on large area devices on N and P MOS devices as a function front gate voltage with body bias Vb=0 for several temperatures down 4.2K (Fig. 2.2). As can be seen, the Cgc(Vg) curves are almost temperature independent above threshold, whereas a strong improvement of the turn-on behaviour is obtained at low temperature, related to the subthreshold slope increase. These characteristics have been well reproduced by Poisson-Schrodinger simulations; providing precise extraction of front oxide EOT values for GO1 and GO2 flavors [2.2] (Modelling details will be given in Deliverable 2.2 due at M12).

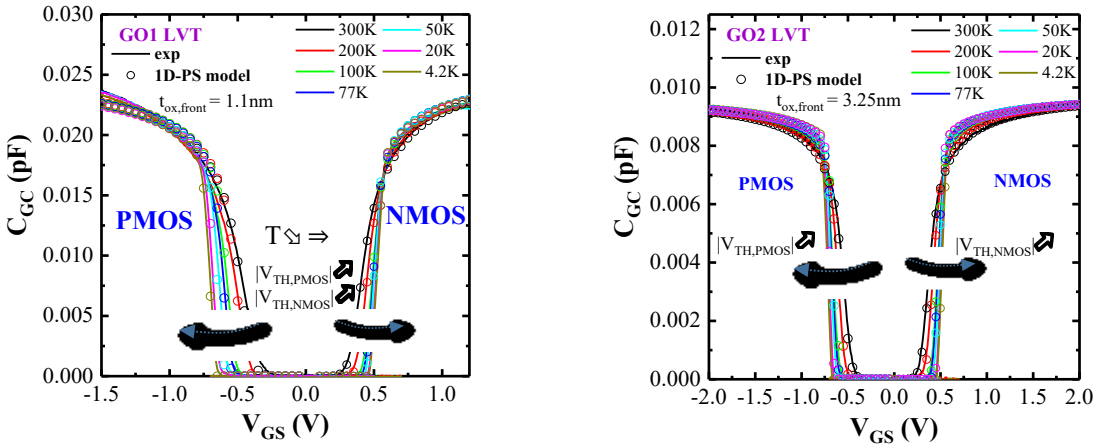


Fig.2.2. *C_{GC} (V_{GS}) characteristics for N- and PMOS GO1 and GO2 devices from 300K down to 4.2K, at V_B = 0V. (Frequency = 1 MHz, AC level = 40mV, W = L = 10µm).*

The influence of the AC level (osc) of the LCR meter oscillator used during Cgc measurements at 4.2K has been studied and is reported in Fig. 2.3a. Indeed, due to the strong non linearity of the Qi(Vg) curves in subthreshold region at very low temperature, the turn-on behaviour of the Cgc(Vg) curve below threshold is not well captured for a too large AC level (here 40mV, currently used at T=300K). However, for an AC level of 1mV, getting closer to the thermal voltage kT/q at 4.2K, the turn-on behaviour of Cgc(Vg) below threshold is well accounted for. These results can be well modelled by integrating over time of one period of AC signal the ideal Ccg(Vg) providing the measured capacitance Cgcmes as follows [2.3]:

$$Cgcmes(Vg) = \frac{1}{Tp}\int_0^{Tp} Cgc\big(Vg + dVg(t)\big)dt \qquad (2.1)$$

where dVg(t)=osc.sin(2πt/Tp) is the AC signal of period Tp (see Fig. 2.3b).

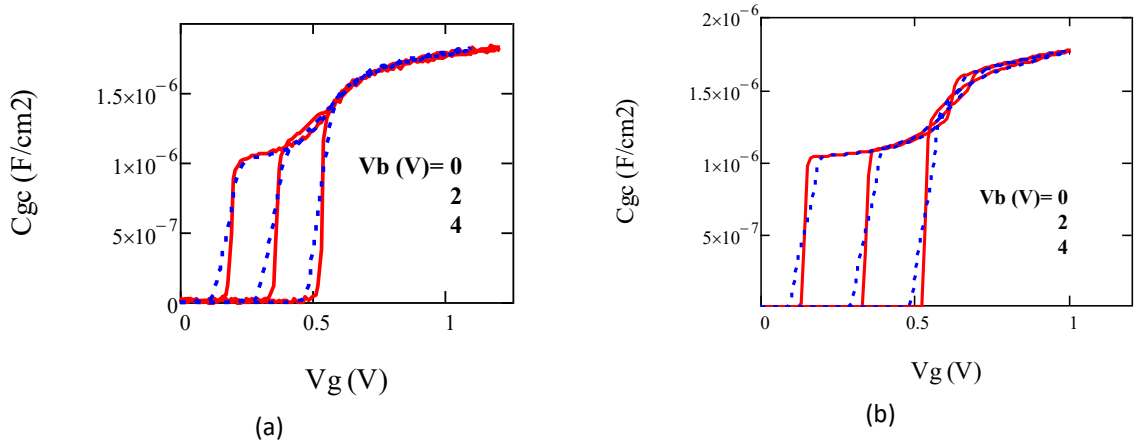


Fig. 2.3. *Experimental (a) and modelled (b) C_{GC} (V_{GS}) characteristics for NMOS GO1 devices (W=L=10µm) at 4.2K for 2 AC levels: 40mV (red solid lines) and 1mV (blue dashed lines).*

2.3 Drain current characteristics, threshold voltage and subthreshold slope

The Id(Vg) transfer characteristics of such devices have been measured in linear region (Vd=50mV) for various temperatures and are shown in Fig. 2.4. As is usual for cryoelectronics in bulk CMOS devices [2.4], the drain current above threshold is significantly increased due to mobility im-

provement resulting from deactivation of phonon scattering, and, the turn-on behavior below threshold is greatly improved as the temperature is lowered.

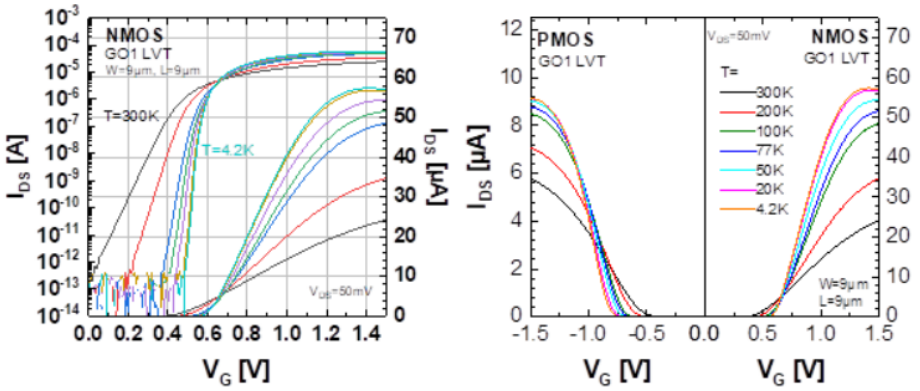


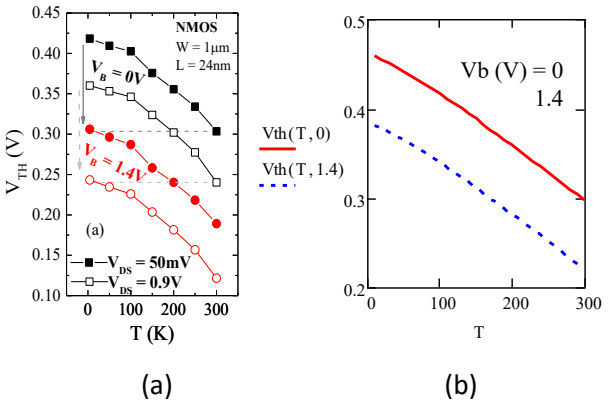
Fig. 2.4. *Id(Vg) characteristics for GO1 N and P MOS devices for various temperatures obtained in linear region (Vd=50mV).*

The threshold voltage of the devices has been extracted by the constant current method (I_D=10^{-7}W/L) and typical variations with temperature are shown in Fig. 2.5a. As is usual [2.4], Vth if found to increase as the temperature is decreased as in bulk MOS devices, here with a sensitivity around 1mV/K. It should be mentioned that in FDSOI devices with undoped film as here, the Vth variation with T are not explained by the temperature dependence of the Fermi level in the silicon film as for bulk MOS devices. Actually, a simple model for Vth read by constant current method can be derived assuming a single subband for the inversion layer with a critical inversion charge density nth as:

$$Vth = Vsth + \frac{q.nth}{Cox} + \frac{Cb.(Vsth - Vb)}{Cox} \tag{2.2}$$

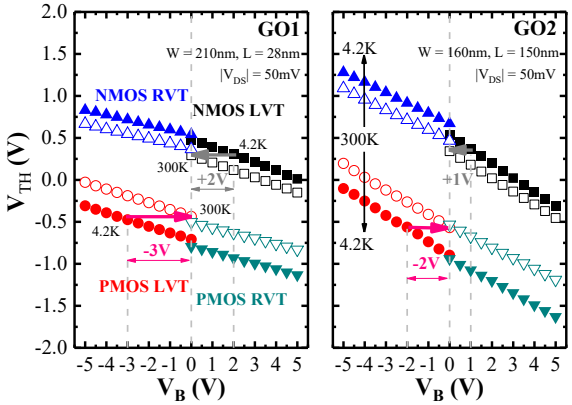
with $Vsth = V0 + \frac{kT}{q}.ln\left(e^{\frac{nth}{kT.A2d}} - 1\right)$ being a threshold surface potential associated with a given constant inversion charge density nth (here 10^{10}/cm^2), and where V0 is a constant and A2d the 2D subband density of states, Cox the front gate oxide capacitance and Cb=Cbox.Csi/(Csi+Cbox) the body to front channel coupling capacitance. As can be seen from Fig. 2.5b a good agreement can be achieved with Eq. 2.2.

An important feature of FDSOI devices is the strong Vth control with the back bias, which is not possible in FinFET and NW architectures, and, very limited in bulk MOS devices [2.4], especially in forward biasing. Typical dependence of Vth with back bias are illustrated in Fig. 2.6 for both P and N MOS FDSOI devices of various flavors GO1 and GO2, and, for T=4.2K and T=300K. As can be seen from this figure, it appears that the threshold voltage control with back biasing is insensitive to temperature down to cryogenic conditions, and, that Vth can be decreased to values close to zero volt. This makes it possible the FDSOI device operation at deep cryogenic temperatures with very small supply voltages (≈0.1-0.2V), enabling low power dissipation.



(a) (b)

Fig. 2.5 *(a) experimental V_{TH} versus T at V_{DS} = 50mV and 0.9V, and at V_B = 0V and 1.4V. (b) modeled Vth vs T for Vd=50mV and Vb=0 and 1.4V.*



(a) (b)

Fig.2.6. *Measurements of V_{TH} vs. V_B for N- and P-type, RVT and LVT, GO1 (a) and GO2 (b) MOSFETs, at 300K and 4.2K, V_{DS} = 50mV.*

Another important parameter in FET operation is the so called subthreshold slope, S=dln(Id)/dVg, or its inverse the subthreshold swing SS, which characterizes the turn-on efficiency of the MOSFET below threshold. Typical subthreshold swing SS (mV/dec) variations with drain current in weak inversion region are shown in Fig. 2.7a, revealing a plateau from which an average subthreshold swing can be extracted and plotted versus temperature (Fig. 2.7b). Indeed, the subthreshold swing SS is varying linearly with temperature down to 25-30K before plateauing around 10-20mV/dec at deep cryogenic temperatures. The SS(T) linear behaviour is usual for all FET devices and simply related to the Maxwell-Boltzmann statistics prevailing in weak inversion where SS=kT/q.(Cox+Cb+Cit)/Cox, Cit being the interface trap density capacitance [2.4]. The SS(T) plateau is generally attributed to the presence of an exponential tail of subband states, likely due to potential-fluctuations-induced disorder [2.5, 2.6, 2.7] and that minimizes the drain current turn-on efficiency at deep cryogenic temperatures.

2.4 Carrier mobility

Finally, the last major parameter of MOSFET operation in linear region is the effective carrier mobility µeff. In Fig. 2.8 a&b are illustrated typical mobility variations with inversion charge Ninv as obtained by split C-V method in such FDSOI MOS devices for various temperatures. As can be seen, there is a strong improvement (up to x10) of the maximum mobility with temperature lowering due to phonon scattering reduction [2.4]. As already found for bulk Si MOSFET [2.4], the effective mobility exhibits a bell-shaped behavior with inversion charge at low temperature [2.4], where the mobility is limited by combined Coulomb and surface roughness scattering processes. As also shown in Fig. 2.8, the mobility can be well fitted by an empirical model inspired from bulk MOSFET results [2.4] and written as:

$$\mu eff = \mu m. \frac{\left(\theta 1.\frac{Qi}{Cox}\right)^{n-2}}{1+\left(\theta 1.\frac{Qi}{Cox}\right)^{n-1}+\left(\theta 2.\frac{Qi}{Cox}\right)^{n}} \quad (2.3)$$

where µm stands for an amplitude mobility value close to the maximum one, θ1 and θ2 are the first and second order attenuation coefficients and n is a power law exponent varying between ≈2 and ≈3 as the temperature is changed from 300K down to 4.2K [2.4], as illustrated in Fig. 2.8c. It should be noted that this mobility law vs inversion charge will be useful for compact modelling purpose (WP2/Task 2.6).

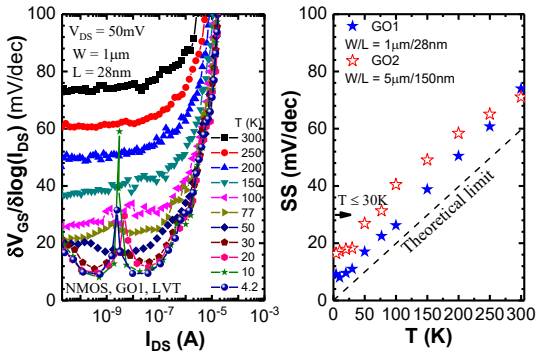


Fig.2.7. *Extracted subthreshold current vs. I_D (a) and SS vs. T (b) for NMOS LVT, from 300K to 4.2K.*

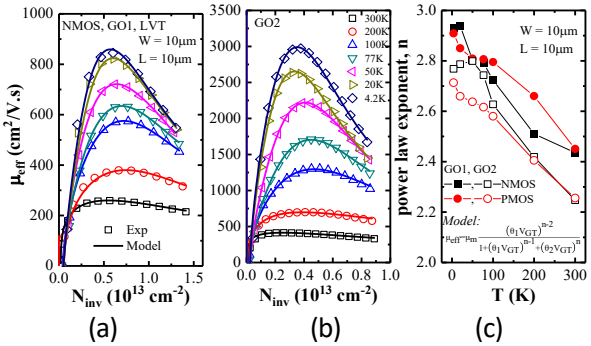
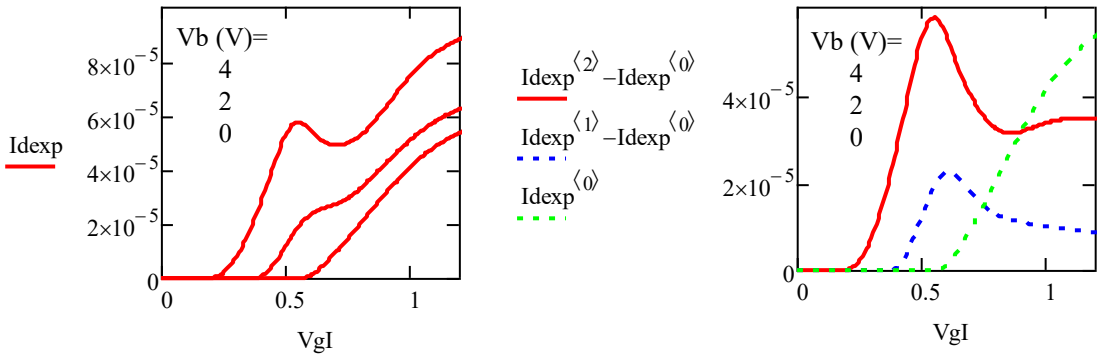


Fig.2.8. *Experiments and analytical model of μ_{eff} vs. N_{inv} for NMOS GO1 (a) and GO2 (b), varying T. Power law exponent (c) vs. T for N and PMOS.*

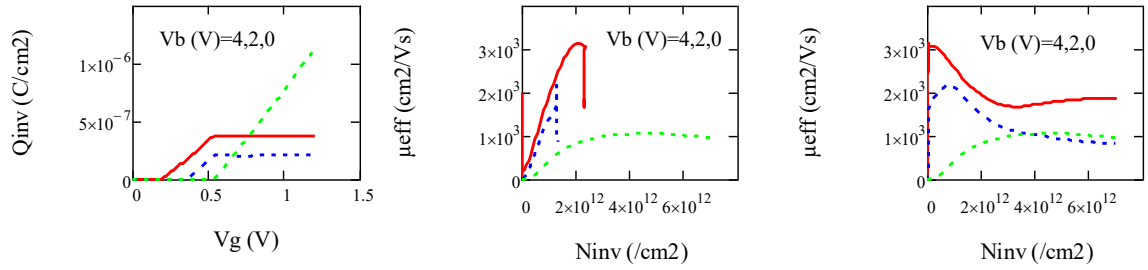
As was already mentioned, a specific feature of FDSOI devices is their operation in forward back biasing condition, enabling a significant lowering of the threshold voltage as illustrated in Fig. 2.9a for T=4.2K. Interestingly, for sufficiently large Vb, the drain current measured at low Vd and very low temperatures (here T=4.2K) is increasing above back channel threshold voltage before to decrease significantly and then to increase again well above front channel threshold. Actually, this decrease of the drain current just happens when the front channel is opening and has been attributed to a reduction of the mobility due to remote intersubband scattering as well explained in [2.8]. To better understand this behavior, we have computed the drain current of the back channel after subtraction of the front channel component, taken as being the one in absence of back channel formation i.e. when Vb=0 (see Fig. 2.9b). This assumption has been validated by Poisson-Schrodinger simulation (not shown here). Doing the same with Cgc(Vg) characteristics for various Vb's, the inversion charge in the back channel has also been computed after integration of capacitance vs Vg as is usual in split C-V technique (Fig. 2.10a). As a result, note that the back channel charge is plateauing after the opening of front channel. The effective mobility in the back channel has been computed and plotted versus inversion charge density in the back channel or the front one as shown in Fig. 2.10b&c. As can be seen, µeff first increases with the back channel inversion charge density before to decrease as the back channel charge saturates (Fig. 2.10b). Instead, µeff in back channel decreases with the front channel inversion charge, which clearly indicates that the opening of the front channel is responsible for the back channel mobility decrease. This is precisely the signature of remote intersubband scattering, which happens when carriers in the back interface 2D subband can interact with the front interface 2D subband. In this situation, some carriers at the back interface can experience scattering mechanisms in the front interface due to the overlap of the back and front subband wave functions. It should be mentioned that this phenomenon of intersubband scattering is cancelling out when the temperatture is increased due to thermal broadening as well as when the drain voltage is increased due to the averaging over the channel of the conductance by integration [2.8].

Finally, it should be noted that this specific intersubband scattering phenomenon has been observed in GO1 and GO2 NMOS devices, but not in PMOS devices (Fig. 2.11).



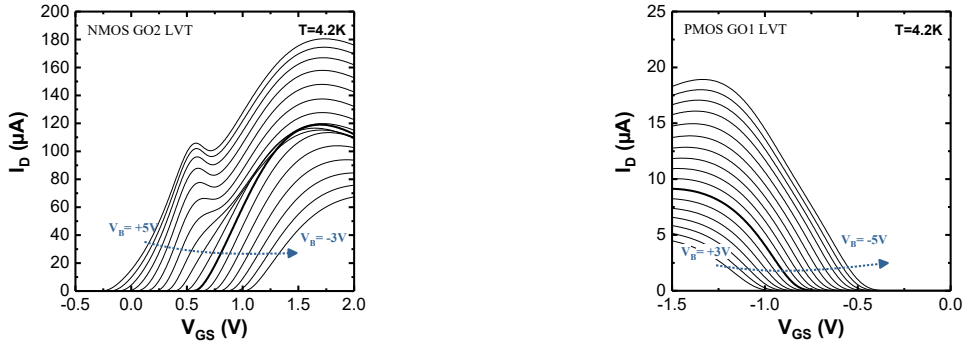
(a) (b)

Fig. 2.9. *a) Id(Vg) characteristics at 4.2K for various Vb (0, 2, 4 V) and b) Back channel Id(Vg) curves after subtraction of front channel component also shown in green dashed line.*



(a) **(b)** **(c)**

Fig. 2.10. *a) Qinv vs Vg for back channel for Vb=2, 4 V. Green curve shows Qinv(Vg) for front channel at Vb=0. b) Back channel µeff vs back channel Ninv and c) back channel µeff vs front channel Ninv for Vb=2, 4V. Green curve shows front channel µeff vs front channel Ninv.*



(a) (b)

Fig. 2.11. *Id(Vg) characteristics at 4.2K for various Vb (from -3V to 5V) for a) NMOS GO2 and b) PMOS GO1 devices. PMOS devices do not exhibit the specific feature whatever Vb.*

3 Characterization of lateral III-V MOS devices (contributor: IBM)

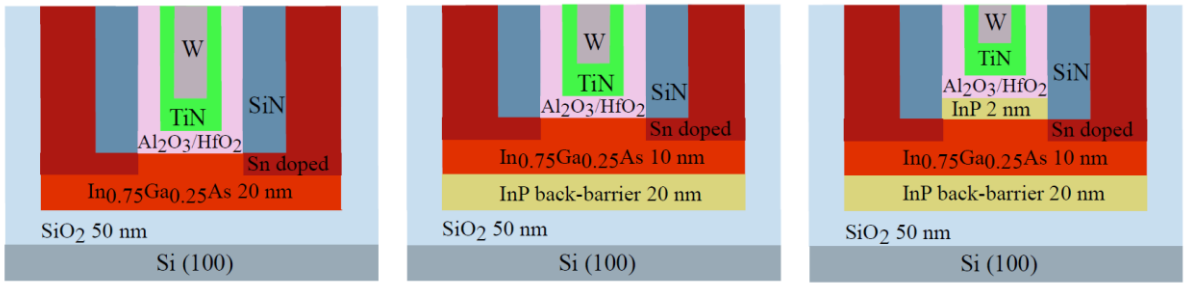


Fig. 3.1. *Schematic figures of the different device structures that were measured. Left shows a standard InGaAs MOSFET with 20 nm thick channel on BOX. In the middle design the channel thickness is reduced to 10 nm and a 20 nm InP back-barrier is added to protect the back-interface. The right-hand side schematic shows a MOSHEMT design with both top and bottom InP barriers and a 10 nm InGaAs quantum well.*

IBM has performed temperature-dependent measurements on III-V lateral transistors fabricated using their CMOS-like process flow [3.1]. Devices were measured down to 4 K using a Janis probe station. The different device structured characterized are shown in figure 3.1. Lefthand side shows an InGaAs MOSFET with 20 nm thick channel integrated on a BOX layer on silicon substrates. In the center device design the channel thickness is reduced to 10 nm and a 20 nm InP back-barrier is added to protect the back-interface. The right-hand side schematic shows a MOSHEMT design with both top and bottom InP barriers and a 10 nm InGaAs quantum well engineered for optimal high-frequency performance. FinFET devices are also characterized and implement the left-hand and middle device designs.

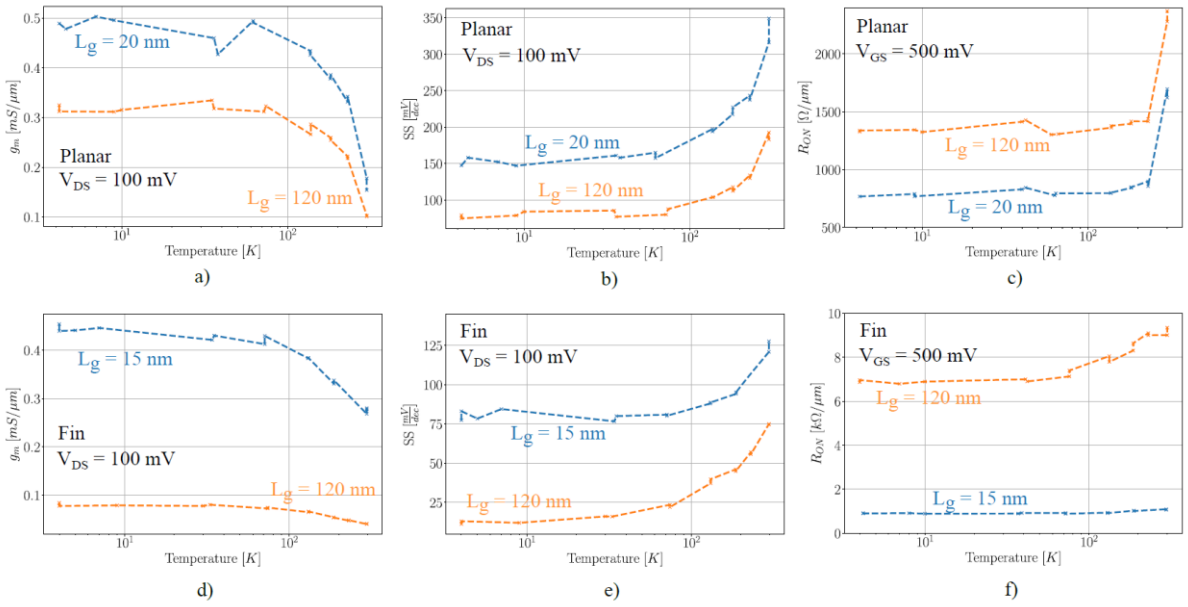


Fig. 3.2. *Measurement data of planar MOSHEMTs (a)-(c) and lateral InGaAs FinFETs (d)-(f). All three metrics, transconductance, subthreshold swing and on-resistance are measured at 100 mV drive bias.*

Figure 3.2 shows measurement data of fabricated devices. Planar MOSHEMTs with gate lengths of 120 and 20 nm are shown in (a)-(c). As seen, transconductance, gm, is relatively equal for the two

gate lengths at room-temperature. At reduced temperatures g_m is significantly increased, from 0.15 and 0.1 mS/µm for 20 and 120 nm, respectively, at room temperature to 0.5 and 0.3 mS/µm at 4 K. On-resistance shows a similar trend. The g_m increase saturates already at around 100 K. Due to measuring at low drive bias, self-heating can be excluded as cause for this saturation. As both gate lengths show approximately the same enhancement of g_m, a factor 3, the effect is likely not due to any change in electrostatics but is rather related to a decrease of scatttering. The FinFET devices (multi-fin around 30 nm wide) also show an increase of g_m, though less pronounced, approximately a factor 1.6. The comparison between the FinFET and planar devices indicates that the MOSHEMTs are to a greater extent limited by phonon scattering in the quantum well (which are thermally activated events), rather than surface scattering at the oxide interfaces. The FinFETs, on the other hand, are limited by surface scattering, which does not show a strong temperature-dependence.

Subthreshold swings for the two device types are also shown. For both types, the short-channel device fails to reach sub-thermionic SS. The planar short-channel device shows 350 mV/decade at room-temperature and is clearly limited by the relatively weak electrostatics due to the reduced gate capacitance from the InP top-barrier. At 4 K, it reaches 150 mV/decade. Neither the long-channel device reaches subthermionic subthreshold swing at 4 K but saturates at around 70 mV/decade. The FinFET devices, however, show significantly stronger electrostatic control, with the long-channel device going from 75 mV/decade to below 20 mV/decade at 4 K. Similar to transconductance, the enhancement of subthreshold swing is strongest down to 100 K, and saturates beyond that temperature. However, it must be noted that the temperature-scale is logarithmic and the expected dependence of the subthreshold swing on the temperature is linear.

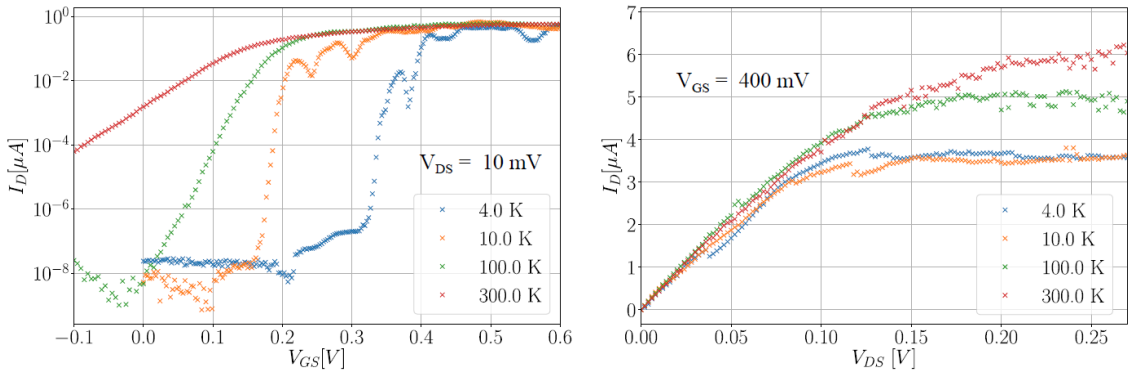


Fig. 3.3. *Transfer and output characteristics of a FinFET with a single 25 nm wide fin.*

In the following, single-fin FinFETs are examined under low-bias conditions. The purpose is to study g_m enhancement due to quantization of energy levels. According to the theory of 1D ballistic FETs, a significant g_m boost can be expected due to the formation of current plateaus in the transfer characteristics **[**3.2**]**. In a scaled ballistic device, i.e. in the quantum capacitance limit, the transconductance is $2q^2/h$. This behavior is remarkable since it exhibits no voltage dependence, indicating that the FET could operate with high gain and low DC power. However, the price comes at linearity, as the g_m becomes progessively narrower as the drive bias is reduced.

Figure 3.3 shows transfer and output characteristics of a FinFET device with a single 25 nm wide fin and with a nominal gate length of around 20 nm (real gate lengths are typically 10-15 nm longer). First, the very sharp increase of the subthreshold swing is noted, going from 75 mV/decade to about 5 mV/decade. Clearly, the reduction is much stronger than for the multi-fin FinFET showed above. Two reasons for this are the reduced drive bias (to 10 mV) and the use of a single fin. Multiple parallel fins in a device can have slight width variations resulting in overlapping transfer curves with slight

threshold voltage V_T variations, essentially averaging out the subthreshold swing. Moreover, there is a huge V_T shift of about 420 mV which is not fully explained by the expected band gap widening for the InGaAs system. The output characteristics show a reduction of the saturation current at V_{GS} = 400 mV, though it must be noted that there are non-linear effects in the transfer characteristics which will influence this result.

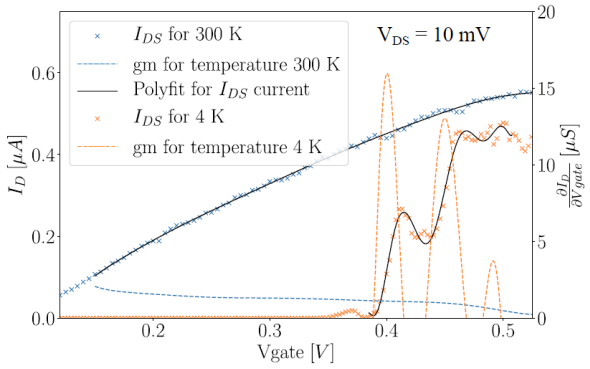


Fig. 3.4. *Study of the transconductance in a single-fin FinFET. Same device as in Fig. 3.3.*

The transconductance of this device is shown in Fig. 3.4. The linear scale transfer characteristics are also shown. Two equidistant steps in the characteristics can be distinguished. Transmission (proportion of ballistic transport) is about 30% here, obtained by plotting the the conductance in terms of conductance quanta. While this behavior could be due to quantized energy levels, further studies would be needed, i.e. measuring of Coulomb diamonds, to verify this. However, it can be seen that there is a large increase of peak transconductance at the current steps. The blue dashed traces show g_m at room-temperature, while the orange traces show at 4 K.

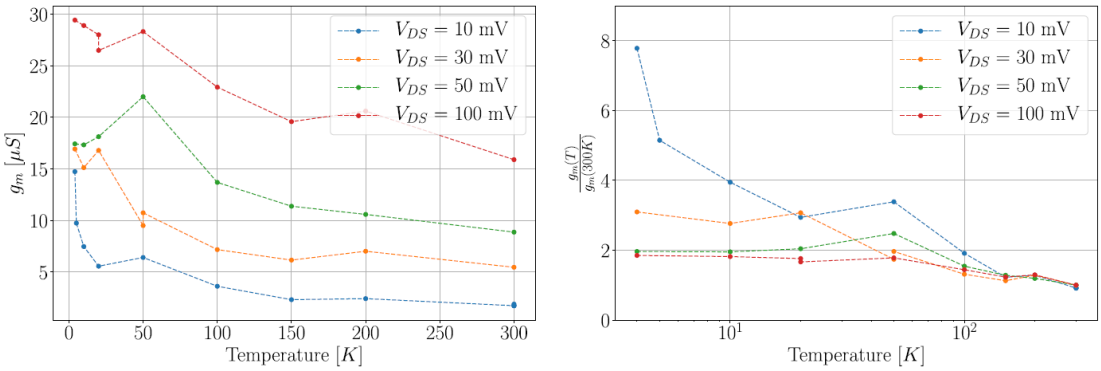


Fig. 3.5. *Study of the transconductance enhancement effect in scaled FinFETs.*

This effect is further shown in Fig. 3.5. The g_m boost is shown in the right-hand figure, and reaches about a factor 8 enhancement at 4 K for 10 mV drive bias. Increased drive bias and temperature significantly lowers the effect. The difference in the behavior of the g_m versus temperature in this single-fin compared to the high-bias multi-fin device indicate that the mechanisms of the g_m enhancement effects are completely different in the two devices. Indeed, the change in the multi-fin device is driven by mobility enhancement, while the change in the single-fin is driven by the sharpening of the Fermi-Dirac distribution.

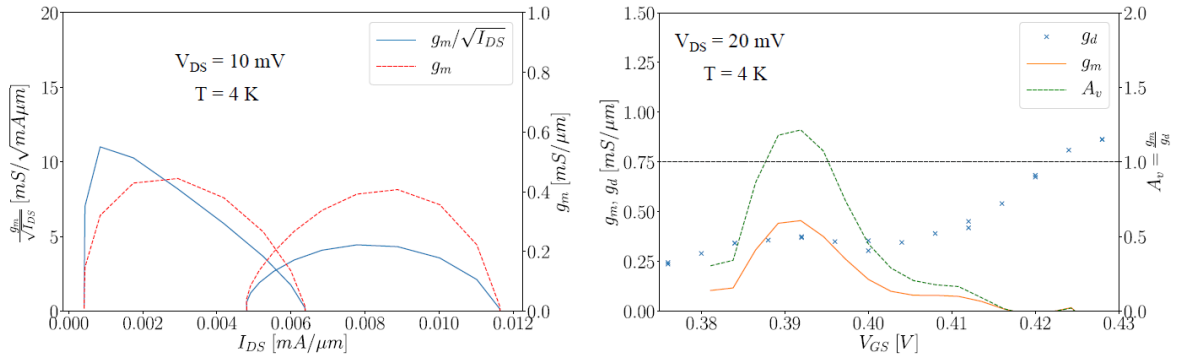


Fig. 3.6. *Left-hand figure shows the gm/VIDS figure of merit, while the righ-hand side shows the voltage gain of the measured device above.*

Finally, a few metrics relating to the application of this type of single-fin quantized FET in an LNA is considered. In an LNA, the minimum noise temperature, which is related to the noise figure, can empirically be described as [3.3]

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{(R_s + R_g + R_{gs})T_g T_d g_d}$$

where f is the operating frequency, f_t is the maximum cut-off frequency, R_s, R_g are the source and gate resistances, R_{gs} is the intrinsic channel resistance, T_g, T_d are the effective gate and drain temperatures and g_d is the output conductance. Outside of the empirical parameters, the minimum noise temperature is minimized by maximizing the function

$$f(V_{GS}, I_{DS}) = \frac{g_m}{\sqrt{I_{DS}}}$$

This function is shown in Fig. 3.6 for the same device as Fig. 3.4 and 3.5. A value of about 10 is reached at 10 mV. It is noted that state-of-the-art standard InP LNAs reach similar values with V_{DD} of above 200 mV. Gm is shown as well to confirm that the function above is maximized around the peak value of g_m, i.e. the feasible operation point of the LNA. Finally, the voltage gain is studied. Since the theory of the 1D FET tells us that also the output conductance g_d is $2q^2/h$, that is the same as the g_m, a voltage gain $A_V = g_m/g_d$ above one may not be expected. However, the measurement does show $A_V = 1.25$ at peak g_m. The reason for this is that g_m and g_d obtain their maximum values at different voltages, as shown in the figure.

4 Temperature-Dependent Characterisation of Vertical III-V Nanowire MOSFETs and TFETs (contributor: ULUND)

4.1 III-V nanowire comparison

ULUND has performed temperature dependent DC electrical characterization of III-V Nanowire MOSFETs and TFETs down to 13 K using a Lakeshore cryogenic probe station. The MOSFETs have 80-160 InAs/InGaAs heterostructure nanowires where the top part and a shell are n-doped. The TFETs have 1-4 InAs/InGaAsSb/GaSb heterostructure nanowires with an undoped InAs channel before the p-doped InGaAsSb source segment (Fig 4.1).

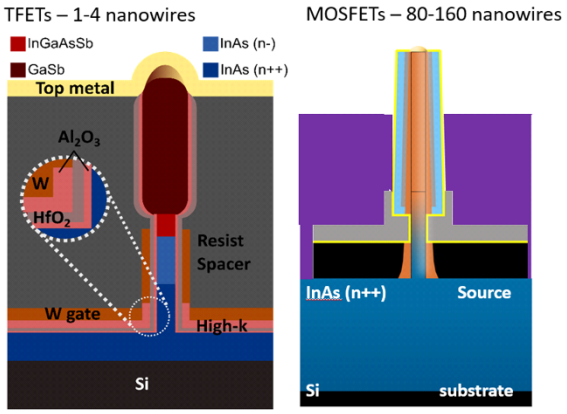


***Fig. 4.1**. Device schematics for InAs/InGaAsSb/GaSb NW TFETs (left) and InAs/InGaAs NW MOSFETs (right).*

The data has been compared with data from a 28 nm silicon on insulator (SOI) process [4.1]. Schematic structures of the measured devices are provided in **Error! Reference source not found.**4.1]. The subthreshold factor *n* according to [4.1] was used as the principal metric to compare devices. In the most general manner, *n* can be defined as a device-dependent prefactor of the inverse subthreshold slope *S* as

$$S = \ln(10)\frac{k_B T}{q}\, n \tag{4.1}$$

with the Boltzmann constant k_B, the temperature *T*, and the elemental charge *q*. It should be noted that this only allows a qualitative comparison at this point, since *n* has different meanings for SOI, III-V MOSFETs, and TFETs. For SOI, *n* is derived from the depletion of the silicon body which is not meaningful for III-V nanowire devices. In addition, III-V devices typically achieve ballistic transport at longer channel lengths than Si, and for TFETs, the expression for *S* is fundamentally different than for MOSFETs. A physical interpretation of the following comparison therefore requires more extensive work.

Fig. 4.2. presents the main results of the comparison. In Fig. **4.2.**(a) it can be seen that *S* in MOSFETs is limited to values above the thermionic limit of $k_B T/q$. At room temperature, TFETs reach significantly lower values than this limit due to the high energy Fermi tail of the electrons in the source being filtered out by the band gap. At temperatures lower than room temperature, the TFETs cannot maintain this performance since the temperature dependence of S is small. At low temperatures *S* eventually saturates at values between 30 and 40 mV/decade, which is even higher than the saturation level of the MOSFETs in this case. A possible explanation for these saturations is the occurrence of so-called band tails extending into the band gap due to doping, defects, or disorder in the semiconductor [4.2]. TFETs are affected by band tails both in the source and in the channel, whereas MOSFETs only suffer from band tails in the channel. In addition, *S* in TFETs can suffer from the occurrence of defects at the tunnel junction [4.3], to which MOSFETs are less sensitive. This could explain the difference between the two kinds of devices.

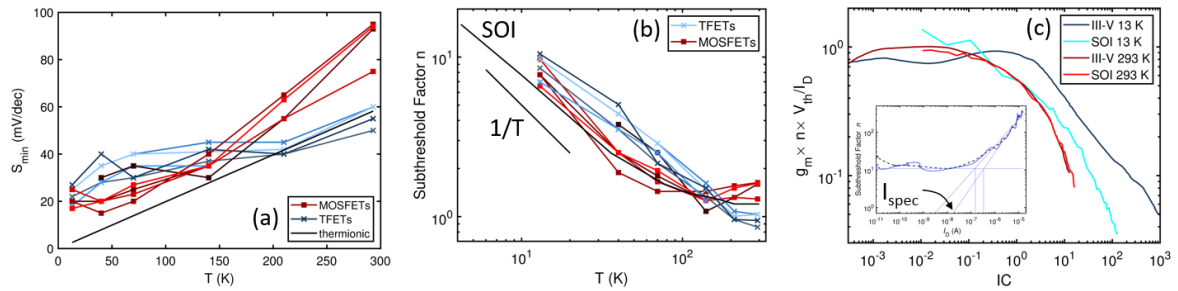
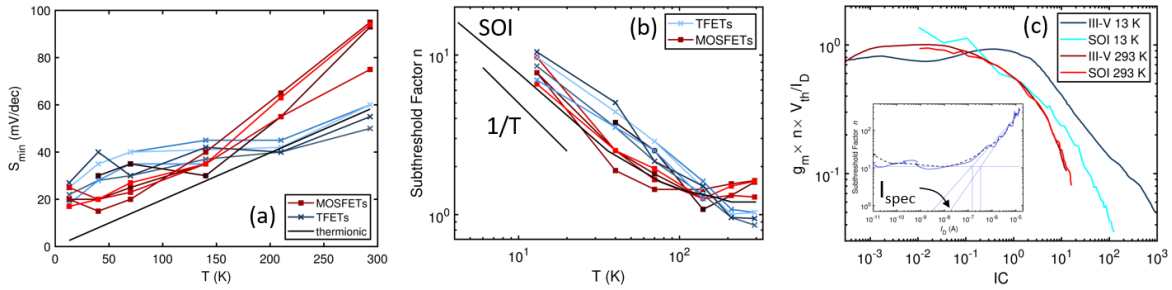


Fig. 4.2. *Comparison as a function of temperature. Red: MOSFETs, blue: TFETs. (a) Minimum inverse subthreshold slope. At room temperature, TFETs reach values below the thermionic limit, but cannot maintain this performance at lower temperatures. (b) Subthreshold factor n. S < 60 mV/decade for TFETs results in n < 1, which is not possible for MOSFETs. (c) Transconductance efficiency normalised with the subthreshold factor. III-V devices in this comparison achieve higher normalised transconductance efficiencies than SOI devices (at most Inversion Coefficients) at low temperatures.*



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The subthreshold factor *n* calculated using the data in Fig. **4.2.**(a) using Eq. (4.1), give $n < 1$ for TFETs at room temperature, which is not possible for MOSFETs or SOI devices. At lower temperatures, *n* for the TFETs increases above the values for MOSFETs and SOI devices. In a more detailed analysis of the physical meaning of *n* for TFETs, this would likely reflect the effect of band tails and defects on the charge transport in TFETs.

Fig. 4.2.(c) compares the normalised transconductance efficiency of III-V MOSFETs with that of SOI devices. The x-axis for this comparison is provided by the Inversion Coefficient I_C, which is defined as $I_C = I_{sat}/I_{spec}$, where I_{sat} is the saturation current of the devices and I_{spec} the so-called specific current, which is determined from the subthreshold factor *n* as demonstrated in the inset of Fig. 4.2.(c). This inset also demonstrates a possible source of error for this comparison, since the calculation of both I_C and *n* is affected by noise in the measurement. Within these margins of error, however, Fig. **4.2.**(c) indicates that III-V devices seem to achieve a higher boost in the transconductance efficiency at low temperatures than SOI devices. This is likely related to the higher mobility in III-V devices and to the corresponding higher ballisticity at similar channel lengths.

4.2 Tunnel FET T-dependent characteristics

The TFET devices have also been studied in more detail by analysing the temperature dependence of the NDR (negative differential resistance) in the forward bias region between 13 K and 300 K. Two different samples have been studied with one having a four times higher Zn doping in the InGaAsSb source segment and MOVPE growth at 20°C higher temperature than the other. The sample with the lower doping is the same as for the analysis of the subthreshold factor described above. The NDR characteristics for a device on the sample with lower doping with different V_{GS} is presented in Fig 4.3. The peak current density is reduced while the thermal current at high V_{SD} is increased with increasing temperature. In contrast, the peak current density for the sample with four times higher source doping exhibits almost no temperature dependence (Fig 4.4) while the thermal current at higher V_{SD} increase with temperature as for the sample with lower doping. The peak current density as a function of temperature for multiple devices is shown in Fig 4.5 together with schematic band structures for a TFET with degenerate and non-degenerate doping. For non-degenerate doping, the Fermi level with shift significantly towards the middle of the band gap with increasing temperature which will reduce the peak current density as observed experimentally (Fig 4.5 middle).

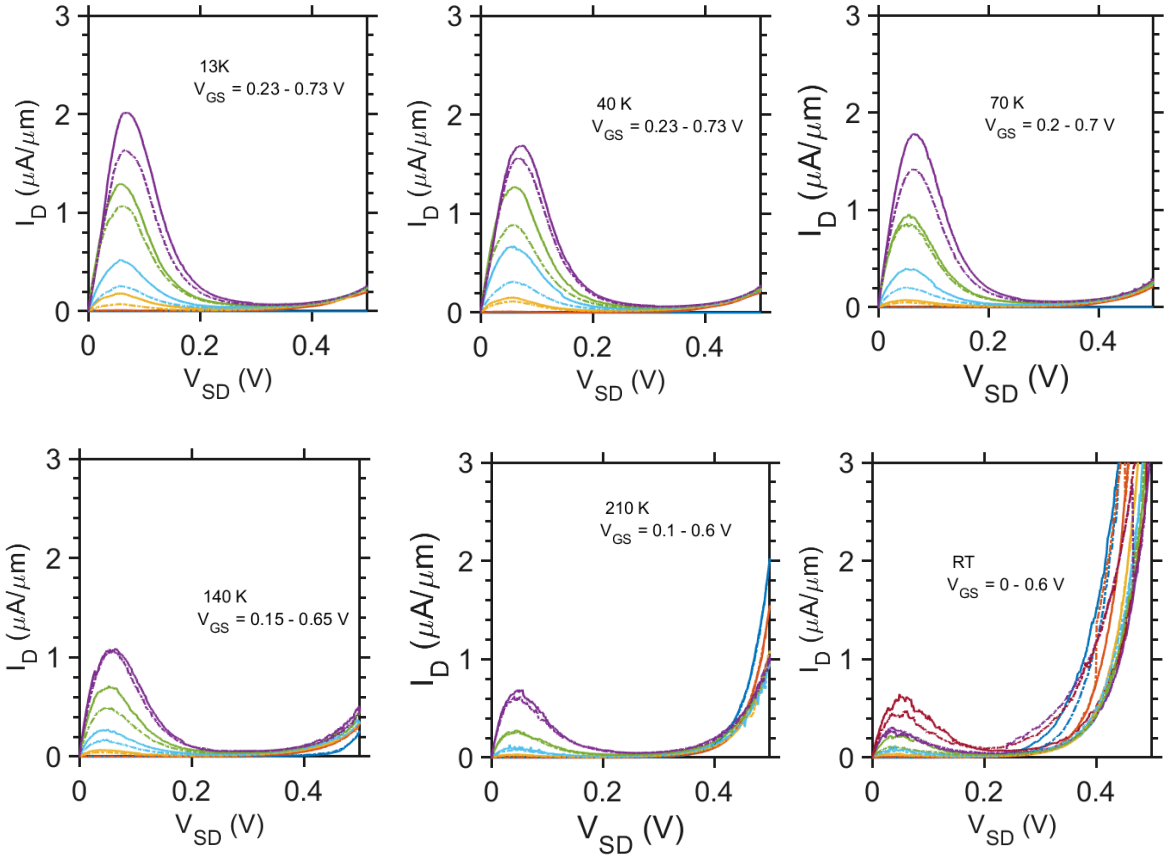

Fig. 4.3: *NDR characteristics of a vertical nanowire TFET device with lower doping at different temperatures.*

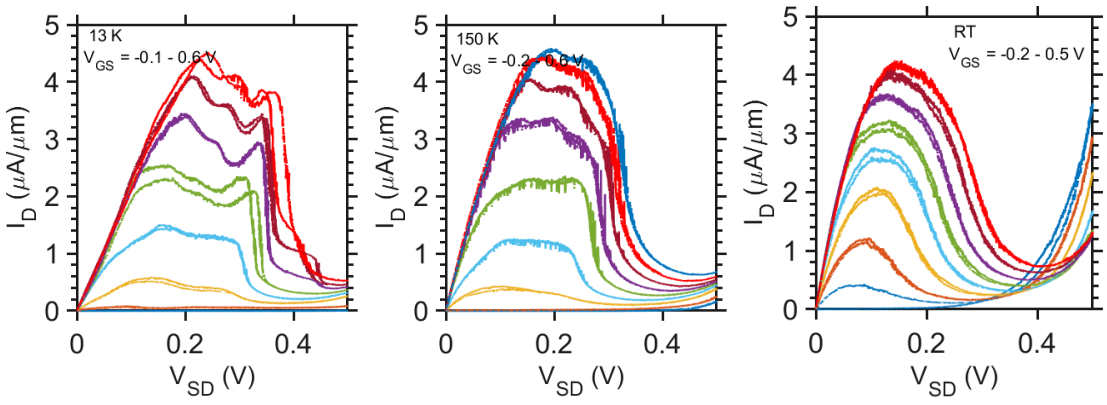

Fig. 4.4: *NDR characteristics of a vertical nanowire TFET device with higher doping at different temperatures.*

For degenerate doping, the shift of the Fermi level towards the middle of the gap with increasing temperature is smaller than for the low doped case. However, since the band gap also decreases with temperature, the resulting tunnelling current is expected to have only little dependence on temperature as is observed experimentally (Fig 4.5 left). The temperature dependent NDR measurements can therefore be used to optimize the source doping since to extensive doping may lead to extended band tails and trap assisted tunnelling deteriorating the subthreshold slope. However, for a reverse biased tunnel junction, which is the region a TFET is normally operated in, the degeneracy has no impact resulting in a temperature independent tunnelling current.

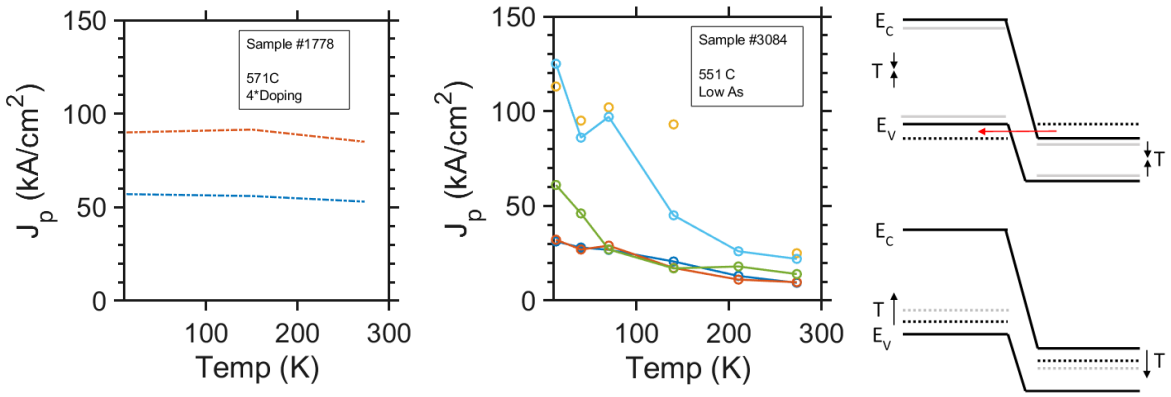

Fig. 4.5: *Peak current density as a function of temperature for a TFET sample (2 devices) with high (left) and a sample (5 devices) with low source doping (middle, 5 devices). Right: Schematic band structure for a TFET with degenerate doping of source and channel and for a TFET with non-degenerate doping.*

For the purpose of integrating III-V nanowire MOSFETs and TFETs into complex circuits, a technology-compatible back-end-of-line (BEOL) has been developed [4.4]. The BEOL is fabricated using a low temperature budget, achieved by using a spin-on benzocyclobutene (BCB) polymer layer cured at 250 °C, enabling efficient planarization of the 3D structures, such as vertical nanowire MOSFETs and TFETs. Interconnects are routed by via dry etching in fluorene plasma and metal evaporation. A schematic cross-section of a full BEOL stack is shown in Fig. 4.6a. It contains 4 metal layers, 3 thick BCB dielectric layers, a thin-film resistor layer and a capacitor layer. The interlayer dielectric is thick to facilitate radio-frequency operation of this BEOL and is optimized for low loss.

Since BCB is a soft polymer layer, its thermal expansion coefficient is rather large (42 ppm/°C [5]), thus ensuring mechanical stability at different temperatures, including cryogenic temperatures, is essential. Fig. 3b shows current-voltage measurements of a stacked via array, as depicted in Fig. 3a. For this measurement, several cryogenic temperatures were used, as well as reference room temperature (300K). As shown in Fig. 4.3b, the resistance is reduced with temperature due to the reduced metal resistivity. Finally, the room temperature measurement is repeated, which gives an identical resistivity as the initial measurement. These measurements show that the via stack, which is a critical connection point in the BEOL stack, remains firmly connected even at 11K. The mechanical stability of the BEOL is thus ensured when used with III-V nanowire MOSFETs and TFETs for realization of cryogenic circuits.

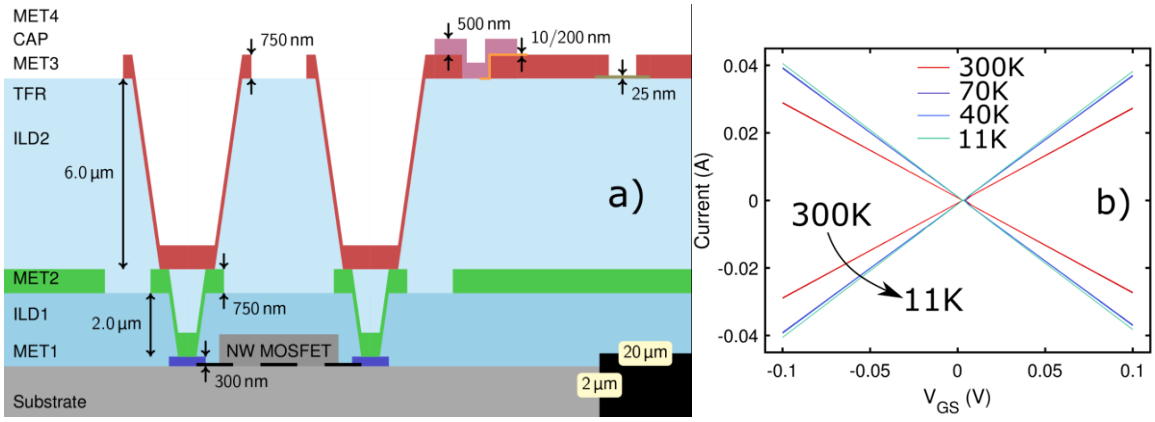

Fig. 4.6: *(a) A schematic cross-section of III-V compatible BEOL with noted metal (METx), interlayer dielectric (ILDx), thin-film resistor (TFR) and capacitor dielectric (CAP) layer, as well as individual height of each of the layers. Via stack is shown as part of device connection. (b) Current-voltage measurements of a via array showing via resistance at room temperature (~300K), 70K, 40K and 11K.*

5 Summary and conclusions

The results obtained by LETI and INPG clearly indicate that 28nm Si FDSOI devices offer very good functionality down to cryogenic temperatures as is the case for bulk Si CMOS devices. However, they provide the unique ability to adjust the threshold voltage by forward back biasing to very low value, enabling the device operation at very low supply voltages (0.1-0.2V) at deep cryogenic temperatures. The subthreshold swing has been found to saturate below 25-30K due to disorder-induced band tail. The mobility under forward bias condition presents a peculiar behaviour attributed to remote intersubband scattering, specific to FDSOI devices with thin enough Si body.

The results from IBM indicate that lateral III-V FinFETs and MOSHEMTs can obtain a strong performance boost at cryogenic temperatures, in particular for the transconductance gain. Two different mechanisms were identified. In MOSHEMTs a strong increase of g_m is observed due to likely reduction of phonon scattering in the quantum well. FinFETs normally showed less of a gm enhancement, though a sharp improvement of the subthreshold swing to below 20 mV/decade was observed. Finally, the concept of a quantized FET towards a low-power cryogenic LNA was studied experimentally. An exceptional transconductance enhancement of a factor 8 was observed showing great promise for this new type of amplifier.

The results from ULUND indicate that III-V nanowire devices should be a suitable alternative for high frequency operation at low temperatures for applications such as control electronics of quan-

tum computers, communication systems, radar and high performance computing. The low temperature operation of TFETs seems to at this point be mainly limited by the presence of band tails and defects in the semiconductor. Therefore, optimization of the source doping is of high importance for improving the performance further.

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